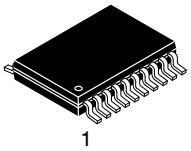
Octal Buffer/Line Driver with 3-State Outputs

74VHC541



TSSOP−20
CASE 948AQ

General Description

The VHC541 is an advanced high−speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high−speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC541 is an octal buffer/line driver designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers.

This device is similar in function to the VHC244 while providing flow−through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

An input protection circuit insures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: t_{PD} = 3.5 ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 4.0 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min)
- Power Down Protection is Provided on All Inputs
- Low Noise: V_{OLP} = 0.9 V (Typ)
- Pin and Function Compatible with 74HC541
- These are Pb−Free Devices

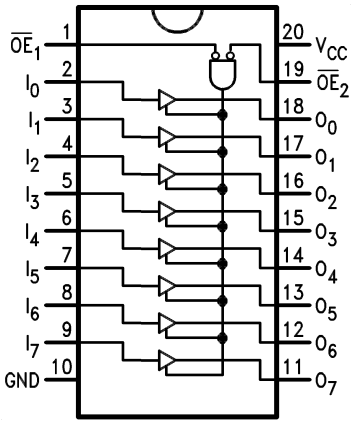


Figure 1. Connection Diagram

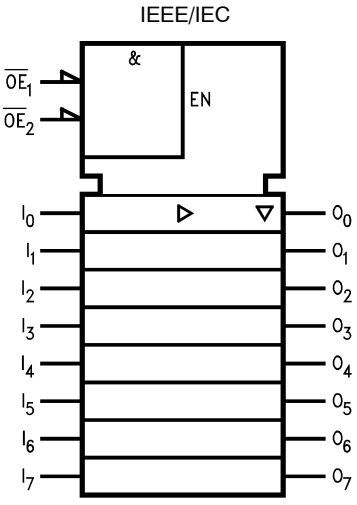
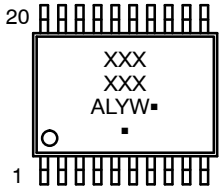


Figure 2. Logic Symbol

MARKING DIAGRAM



XXXXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN DESCRIPTIONS

PIN NAME	DESCRIPTIONS
$\overline{OE}_1$, $\overline{OE}_2$	3−STATE Output Enable Inputs
$I_0 - I_7$	Inputs
$O_0 - O_7$	3−STATE Outputs

TRUTH TABLE

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC}+0.5	V
I_{IN}	DC Input Current		±20	mA
I_{OUT}	DC Output Current		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 s		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)		150	°C/W
P_D	Power Dissipation in Still Air at 25°C		833	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.540 in	–
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage (Note 4)		0	5.5	V
V_{OUT}	DC Output Voltage (Note 4)		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 3.0 V to 3.6 V V_{CC} = 4.5 V to 5.5 V	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	LOW Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OH} = −50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = −4 mA I_{OH} = −8 mA	 3.0 4.5	 2.58 3.94			 2.48 3.80		
V_{OL}	LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4 mA I_{OL} = 8 mA	 3.0 4.5			 0.36 0.36		 0.44 0.44	
I_{OZ}	3−STATE Output Off−State Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	5.5			±0.25		±2.5	μA
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOISE CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C		Unit
				Typ	Max	
V_{OLP} (Note 5)	Quiet Output Maximum Dynamic V_{OL}	C_L = 50 pF	5.0	0.9	1.2	V
V_{OLV} (Note 5)	Quiet Output Minimum Dynamic V_{OL}	C_L = 50 pF	5.0	−0.8	−1.0	V
V_{IHD} (Note 5)	Minimum HIGH Level Dynamic Input Voltage	C_L = 50 pF	5.0		3.5	V
V_{ILD} (Note 5)	Maximum LOW Level Dynamic Input Voltage	C_L = 50 pF	5.0		1.5	V

5. Parameter guaranteed by design.

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C			T_A = − 40°C to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Time	C_L = 15 pF	3.3 ±0.3		5.0	7.0	1.0	8.5	ns
		C_L = 50 pF			7.5	10.5	1.0	12.0	
		C_L = 15 pF	5.0 ±0.5		3.5	5.0	1.0	6.0	
		C_L = 50 pF			5.0	7.0	1.0	8.0	
t_{PZL}, t_{PZH}	3−STATE Output Enable TIme	R_L = 1 kΩ C_L = 15 pF	3.3 ±0.3		6.8	10.5	1.0	12.5	ns
		C_L = 50 pF			9.3	14.0	1.0	16.0	
		R_L = 1 kΩ C_L = 15 pF	5.0 ±0.5		4.7	7.2	1.0	8.5	
		C_L = 50 pF			6.2	9.2	1.0	10.5	
t_{PLZ}, t_{PHZ}	3−STATE Output Disable Time	R_L = 1 kΩ C_L = 50 pF	3.3 ±0.3		11.2	15.4	1.0	17.5	ns
		R_L = 1 kΩ C_L = 50 pF	5.0 ±0.5		6.0	8.8	1.0	10.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	(Note 6) C_L = 50 pF	3.3 ±0.3			1.5		1.5	ns
		(Note 6) C_L = 50 pF	5.0 ±0.5			1.0		1.0	ns
C_{IN}	Input Capacitance	V_{CC} = Open			4	10		10	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0 V			6				pF
C_{PD}	Power Dissipation Capacitance	(Note 7)			18				pF

6. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|$; $t_{OSHL} = |t_{PHLmax} - t_{PHLmin}|$.
7. CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (OPR.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/8 (per bit).

ORDERING INFORMATION

Device	Marking	Package	Shipping†
74VHC541MTC	VHC 541	TSSOP−20	75 Units / Tube
74VHC541MTCX	VHC 541	TSSOP−20	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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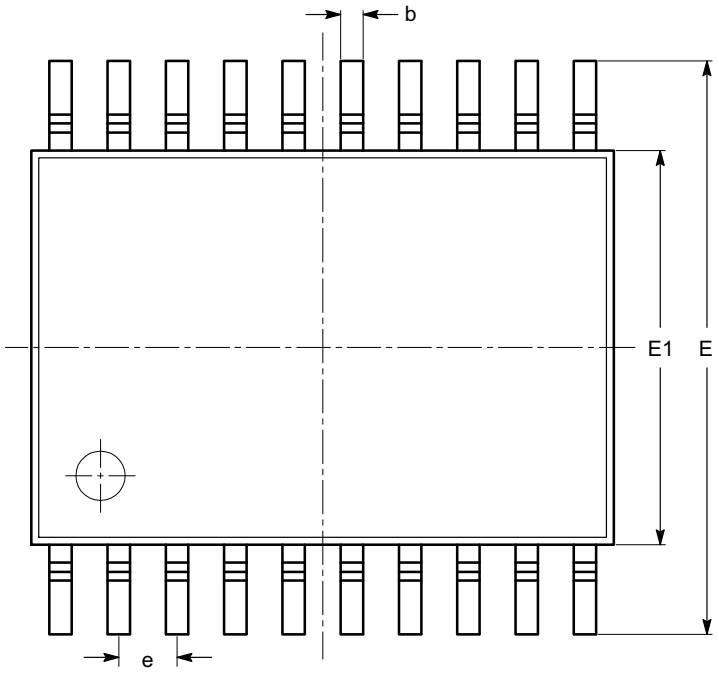
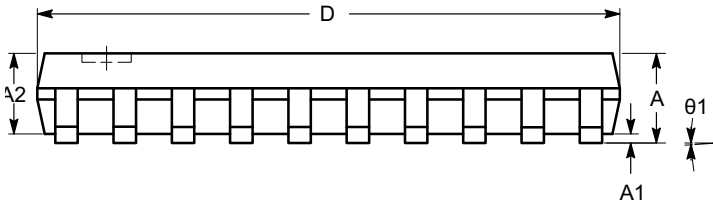
CASE 948AQ
ISSUE A

DATE 19 MAR 2009

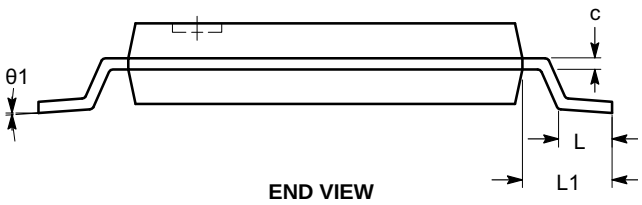


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

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