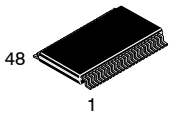
# Low-Voltage 16-Bit Buffer/Line Driver with 5 V Tolerant Inputs and Outputs

# 74LCX16244




**TSSOP48 12.5x6.1**
**CASE 948BQ**

## General Description

The LCX16244 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The LCX16244 is designed for low voltage (2.5 or 3.3 V) $V_{CC}$ applications with capability of interfacing to a 5 V signal environment.

The LCX16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

## Features

- 5 V Tolerant Inputs and Outputs
- 1.65 V to 5.5 V $V_{CC}$ Specifications Provided
- 4.5 ns $t_{PD}$ max ($V_{CC}$ = 3.3 V)
- 10 μA $I_{CCQ}$ max
- Power Down High Impedance Inputs and Outputs
- Supports Live Insertion and Withdrawal*
- ±24 mA Output Drive ($V_{CC}$ = 3.0 V)
- Uses Patented Noise/EMI Reduction Circuitry
- Latch-up Performance Exceeds 100 mA
- ESD Performance:
  - ♦ Human Body Model >2000 V
- This Device is Halide Free and Pb-Free

* To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

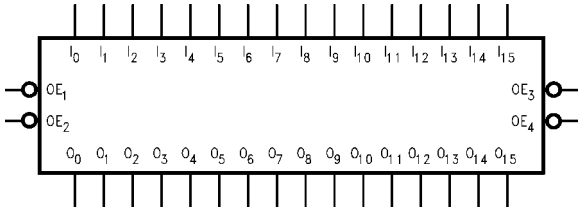



**Figure 1. Logic Symbol**

## MARKING DIAGRAM

| | |
|---|---|
| LCX16244 | = Specific Device Code |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| $\overline{OE}_n$ | Output Enable Input (Active LOW) |
| $I_0$–$I_{15}$ | Inputs |
| $O_0$–$O_{15}$ | Outputs |
| NC | No Connect |

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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### Connection Diagram

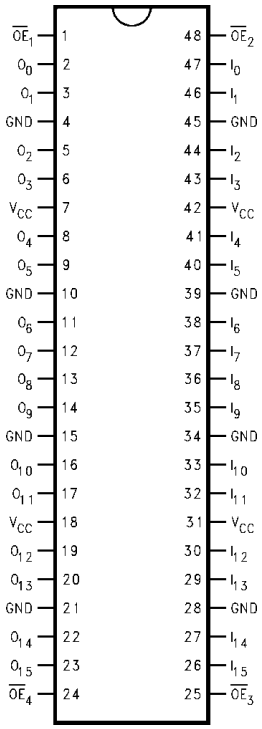


**Figure 2. Pin Assignment**

### TRUTH TABLE

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_1$ | $I_0$-$I_3$ | $O_0$-$O_3$ |
| L | L | L |
| L | H | H |
| H | X | Z |

| $\overline{OE}_2$ | $I_4$-$I_7$ | $O_4$-$O_7$ |
|---|---|---|
| L | L | L |
| L | H | H |
| H | X | Z |

| $\overline{OE}_3$ | $I_8$-$I_{11}$ | $O_8$-$O_{11}$ |
|---|---|---|
| L | L | L |
| L | H | H |
| H | X | Z |

| $\overline{OE}_4$ | $I_{12}$-$I_{15}$ | $O_{12}$-$O_{15}$ |
|---|---|---|
| L | L | L |
| L | H | H |
| H | X | Z |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

### Functional Description

The LCX16244 contains sixteen non-inverting buffers with 3-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

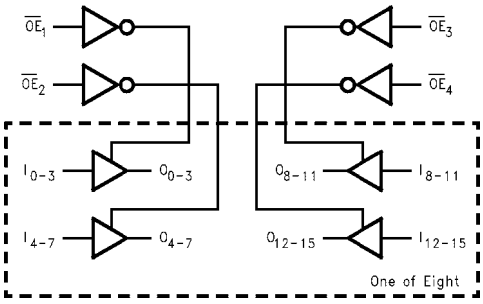


**Figure 3. Logic Diagram**



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## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | –0.5 to +6.5 | V |
| $V_{IN}$ | DC Input Voltage (Note 1) | | –0.5 to +6.5 | V |
| $V_{OUT}$ | DC Output Voltage (Note 1)<br>Tri-State Mode<br>Power-Down Mode ($V_{CC}$ = 0 V) | Active-Mode (High or Low State) | –0.5 to $V_{CC}$ + 0.5<br>–0.5 to +6.5<br>–0.5 to +6.5 | V |
| $I_{IK}$ | DC Input Diode Current | $V_{IN}$ < GND | –50 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_{OUT}$ < GND | –50 | mA |
| $I_O$ | DC Output Source/Sink Current | | ±50 | mA |
| $I_{CC}$ | DC Supply Current per Supply Pin | | ±100 | mA |
| $I_{GND}$ | DC Supply Current per Ground Pin | | ±100 | mA |
| $T_{STG}$ | Storage Temperature Range | | –65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 secs | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 2) | | 71 | °C/W |
| $P_D$ | Power Dissipation in Still Air | | 1765 | mW |
| MSL | Moisture Sensitivity | | Level 1 | – |
| $F_R$ | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | – |
| $V_{ESD}$ | ESD Withstand Voltage (Note 3)<br>Charged Device Model | Human Body Model | >2000<br>N/A | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $I_O$ absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage<br>Data Retention Only | Operating | 1.65<br>1.5 | 3.3<br>3.3 | 5.5<br>5.5 | V |
| $V_{IN}$ | Digital Input Voltage (Note 4) | | 0 | – | 5.5 | V |
| $V_{OUT}$ | Output Voltage (Note 4)<br>Tri-State Mode<br>Power Down Mode ($V_{CC}$ = 0 V) | Active Mode (High or Low State) | 0<br>0<br>0 | –<br>–<br>– | $V_{CC}$<br>5.5<br>5.5 | V |
| $T_A$ | Operating Free-Air Temperature | | –55 | – | +125 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Rate<br>$V_{CC}$ = 2.3 V to 2.7 V<br>$V_{IN}$ from 0.8 V to 2.0 V, $V_{CC}$ = 3.0 V<br>$V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ = 1.65 V to 1.95 V | 0<br>0<br>0<br>0 | –<br>–<br>–<br>– | 20<br>20<br>10<br>5 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.



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## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = −40 °C to +85 °C | | $T_A$ = −55 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $V_{IH}$ | High-Level Input Voltage | | 1.65 to 1.95 | 0.65 x $V_{CC}$ | – | 0.65 x $V_{CC}$ | – | V |
| | | | 2.3 to 2.7 | 1.7 | – | 1.7 | – | |
| | | | 2.7 to 3.6 | 2.0 | – | 2.0 | – | |
| | | | 4.5 to 5.5 | 0.7 x $V_{CC}$ | – | 0.7 x $V_{CC}$ | – | |
| $V_{IL}$ | Low-Level Input Voltage | | 1.65 to 1.95 | – | 0.35 x $V_{CC}$ | – | 0.35 x $V_{CC}$ | V |
| | | | 2.3 to 2.7 | – | 0.7 | – | 0.7 | |
| | | | 2.7 to 3.6 | – | 0.8 | – | 0.8 | |
| | | | 4.5 to 5.5 | – | 0.3 x $V_{CC}$ | – | 0.3 x $V_{CC}$ | |
| $V_{OH}$ | High-Level Output Voltage | $V_I$ = $V_{IH}$<br>$I_{OH}$ = −100 μA<br>$I_{OH}$ = −4 mA<br>$I_{OH}$ = −8 mA<br>$I_{OH}$ = −12 mA<br>$I_{OH}$ = −16 mA<br>$I_{OH}$ = −24 mA<br>$I_{OH}$ = −32 mA | <br>1.65 to 5.5<br>1.65<br>2.3<br>2.7<br>3.0<br>3.0<br>4.5 | <br>$V_{CC}$ − 0.1<br>1.2<br>1.8<br>2.2<br>2.4<br>2.2<br>3.8 | <br>–<br>–<br>–<br>–<br>–<br>–<br>– | <br>$V_{CC}$ − 0.1<br>1.2<br>1.8<br>2.2<br>2.4<br>2.2<br>3.8 | <br>–<br>–<br>–<br>–<br>–<br>–<br>– | V |
| $V_{OL}$ | Low-Level Output Voltage | $V_I$ = $V_{IL}$<br>$I_{OL}$ = 100 μA<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 8 mA<br>$I_{OL}$ = 12 mA<br>$I_{OL}$ = 16 mA<br>$I_{OL}$ = 24 mA<br>$I_{OL}$ = 32 mA | <br>1.65 to 5.5<br>1.65<br>2.3<br>2.7<br>3.0<br>3.0<br>4.5 | <br>–<br>–<br>–<br>–<br>–<br>–<br>– | <br>0.1<br>0.45<br>0.6<br>0.4<br>0.4<br>0.55<br>0.6 | <br>–<br>–<br>–<br>–<br>–<br>–<br>– | <br>0.1<br>0.45<br>0.6<br>0.4<br>0.4<br>0.55<br>0.6 | V |
| $I_I$ | Input Leakage Current | $V_I$ = 0 to 5.5 V | 3.6 | – | ±5.0 | – | ±5.0 | μA |
| $I_{OZ}$ | 3-State Output Leakage Current | $V_I$ = $V_{IH}$ or $V_{IL}$, $V_O$ = 0 V to 5.5 V | 3.6 | – | ±5.0 | – | ±5.0 | μA |
| $I_{OFF}$ | Power Off Leakage Current | $V_I$ = 5.5 V or $V_O$ = 5.5 V | 0 | – | 10 | – | 10 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_I$ = 5.5 V or GND | 3.6 | – | 10 | – | 10 | μA |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | $V_{IH}$ = $V_{CC}$ − 0.6 V | 2.3 to 3.6 | – | 500 | – | 500 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



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## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Condition | $V_{CC}$ (V) | $T_A$ = −40 °C to +85 °C | | $T_A$ = −55 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, I to O | See Figures 4 and 5 | 1.65 to 1.95 | – | 8.5 | – | 8.5 | ns |
| | | | 2.3 to 2.7 | – | 5.4 | – | 5.4 | |
| | | | 2.7 | – | 5.2 | – | 5.2 | |
| | | | 3.0 to 3.6 | – | 4.5 | – | 4.5 | |
| | | | 4.5 to 5.5 | – | 4.0 | – | 4.0 | |
| $t_{PZH}$, $t_{PZL}$ | Output Enable Time, $\overline{OE}$ to O | See Figures 4 and 5 | 1.65 to 1.95 | – | 10.5 | – | 10.5 | ns |
| | | | 2.3 to 2.7 | – | 7.2 | – | 7.2 | |
| | | | 2.7 | – | 6.3 | – | 6.3 | |
| | | | 3.0 to 3.6 | – | 5.5 | – | 5.5 | |
| | | | 4.5 to 5.5 | – | 5.5 | – | 5.5 | |
| $t_{PHZ}$, $t_{PLZ}$ | Output Disable Time, $\overline{OE}$ to O | See Figures 4 and 5 | 1.65 to 1.95 | – | 9.7 | – | 9.7 | ns |
| | | | 2.3 to 2.7 | – | 6.5 | – | 6.5 | |
| | | | 2.7 | – | 5.7 | – | 5.7 | |
| | | | 3.0 to 3.6 | – | 5.4 | – | 5.4 | |
| | | | 4.5 to 5.5 | – | 5.4 | – | 5.4 | |
| $t_{OSHL}$, $t_{OSLH}$ | Output to Output Skew, (Note 5) | | 1.65 to 1.95 | – | – | – | – | ns |
| | | | 2.3 to 2.7 | – | – | – | – | |
| | | | 2.7 | – | – | – | – | |
| | | | 3.0 to 3.6 | – | 1.0 | – | 1.0 | |
| | | | 4.5 to 5.5 | – | – | – | – | |

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) ot LOW-to-HIGH ($t_{OSLH}$).

## DYNAMIC SWITCHING CHARACTERISTICS (Note 6)

| Symbol | Characteristic | Condition | $V_{CC}$ (V) | $T_A$ = +25 °C, Typical | Units |
|---|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Dynamic Peak $V_{OL}$ | $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V<br>$C_L$ = 30 pF, $V_{IH}$ = 2.5 V, $V_{IL}$ = 0 V | 3.3<br>2.5 | 0.8<br>0.6 | V |
| $V_{OLV}$ | Quiet Output Dynamic Valley $V_{OL}$ | $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V<br>$C_L$ = 30 pF, $V_{IH}$ = 2.5 V, $V_{IL}$ = 0 V | 3.3<br>2.5 | −0.8<br>−0.6 | V |

6. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

## CAPACITANCE

| Symbol | Parameter | Condition | Typical | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | VCC = Open, VI = 0 V or VCC | 7 | pF |
| $C_{OUT}$ | Output Capacitance | VCC = 3.3 V, VI = 0 V or VCC | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 7) | VCC = 3.3 V, VI = 0 V or VCC, f = 10 MHz | 20 | pF |

7. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. $C_{PD}$ is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.



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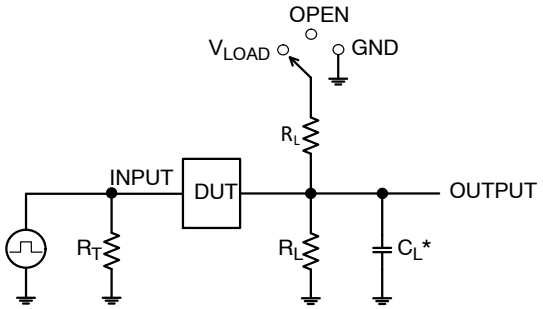
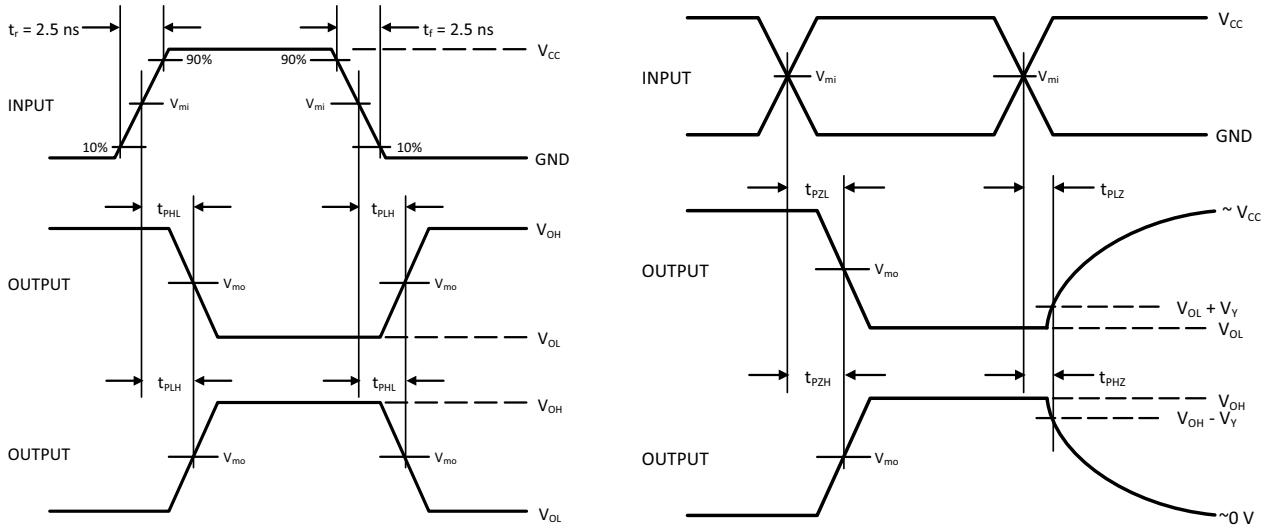



| Test | Switch Position |
|---|---|
| $t_{PLH}$ / $t_{PHL}$ | Open |
| $t_{PLZ}$ / $t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}$ / $t_{PZH}$ | GND |

$C_L$ includes probe and jig capacitance
$R_T$ is $Z_{OUT}$ of pulse generator (typically 50 Ω)
f = 1 MHz

**Figure 4. Test Circuit**




| $V_{CC}$, V | $R_L$, Ω | $C_L$, pF | $V_{LOAD}$ | $V_{mi}$, V | $V_{mo}$, V | $V_Y$, V |
|---|---|---|---|---|---|---|
| 1.65 to 1.95 | 500 | 30 | 2 x $V_{CC}$ | $V_{CC}$/2 | $V_{CC}$/2 | 0.15 |
| 2.3 to 2.7 | 500 | 30 | 2 x $V_{CC}$ | $V_{CC}$/2 | $V_{CC}$/2 | 0.15 |
| 2.7 | 500 | 50 | 6 V | 1.5 | 1.5 | 0.3 |
| 3.0 to 3.6 | 500 | 50 | 6 V | 1.5 | 1.5 | 0.3 |
| 4.5 to 5.5 | 500 | 50 | 2 x $V_{CC}$ | $V_{CC}$/2 | $V_{CC}$/2 | 0.3 |

**Figure 5. Switching Waveforms**



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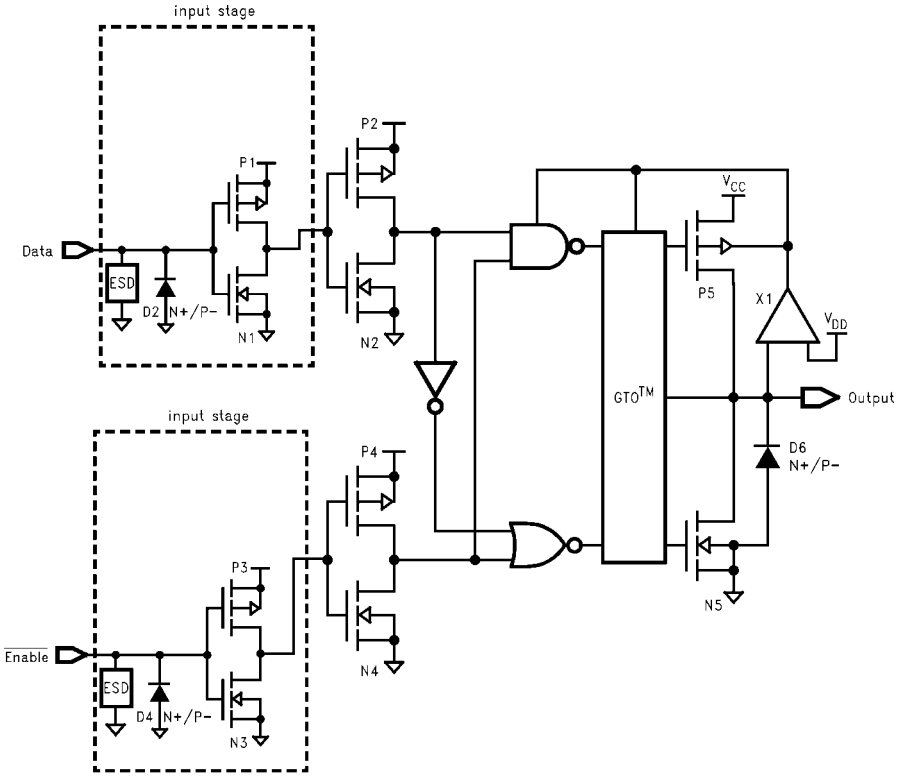


**Figure 6. Schematic Diagram**

## ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| 74LCX16244MTDX | LCX16244G | TSSOP-48 | 1,000 Units / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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## REVISION HISTORY

| Revision | Description of Changes | Date |
|---|---|---|
| 1 | Converted the Data Sheet to **onsemi** format with the updates in Ordering Information Table, Recommended Operating Table, Maximum Rating Table and Figure 4 and 5 from the data sheet MC74LCX16244/D. | 9/29/2025 |
| 2 | Added electrical characteristics for TBD specifications and made editorial corrections throughout the document. | 3/6/2026 |

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



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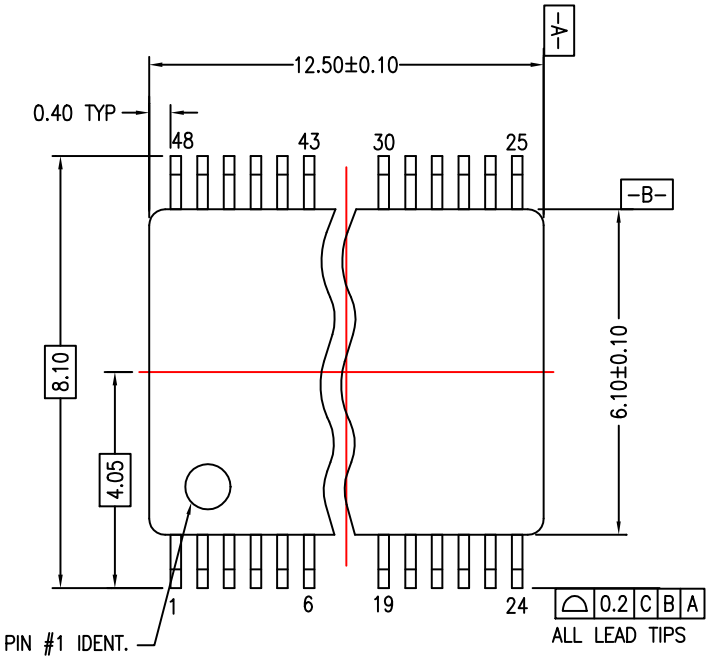
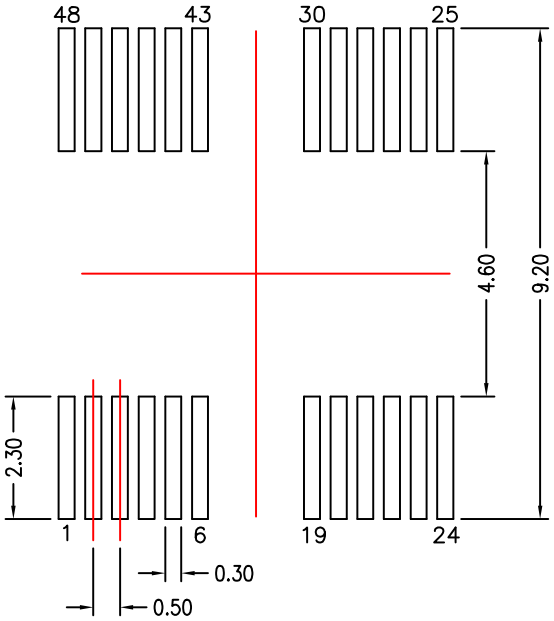
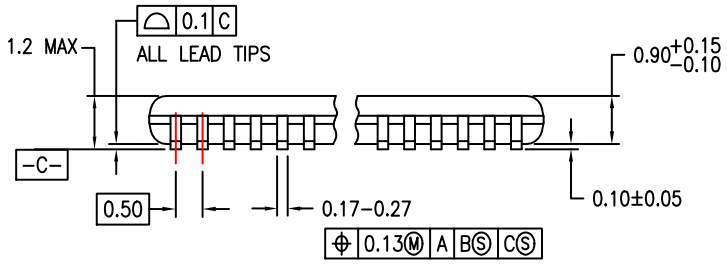
**TSSOP48 12.5x6.1**
CASE 948BQ
ISSUE O

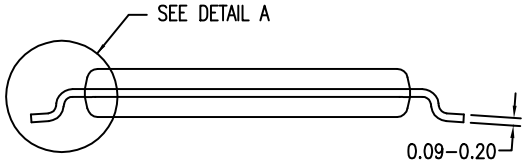
DATE 30 SEP 2016

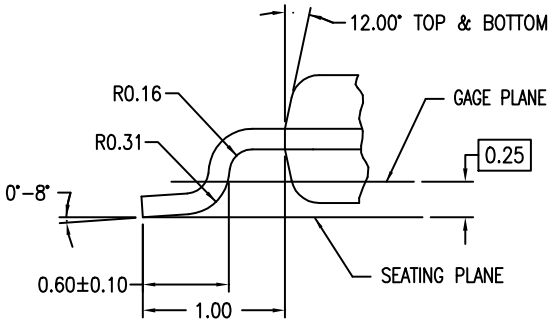



LAND PATTERN RECOMMENDATION




DETAIL A

DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−153, VARIATION ED, DATE 4/97.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

| | | | |
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