

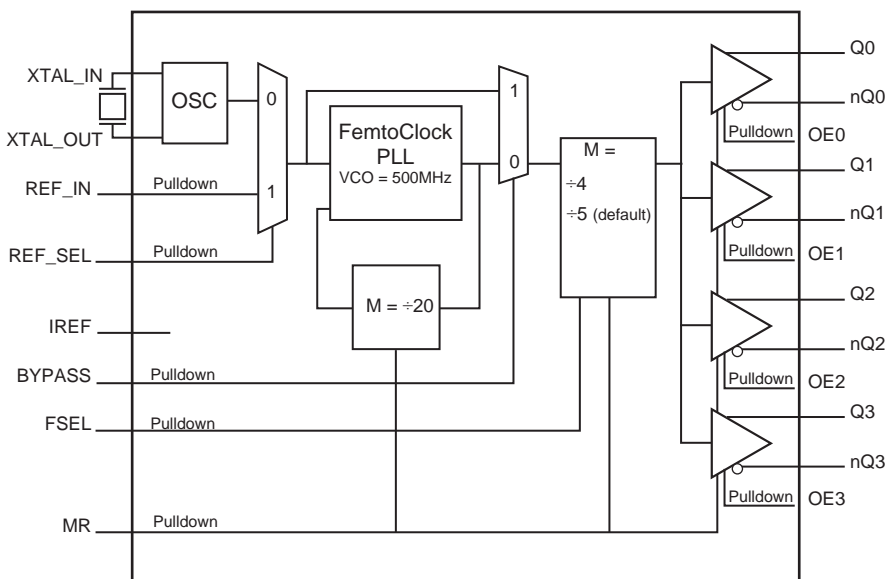
General Description

The ICS841604I-01 is an optimized PCIe and sRIO clock generator. The device uses a 25MHz parallel crystal to generate 100MHz and 125MHz clock signals, replacing solutions requiring multiple oscillator and fanout buffer solutions. The device has excellent phase jitter (< 1ps rms) suitable to clock components requiring precise and low-jitter PCIe or sRIO or both clock signals. Designed for telecom, networking and industrial applications, the ICS841604I-01 can also drive the high-speed sRIO and PCIe SerDes clock inputs of communication processors, DSPs, switches and bridges.

Features

- Four 0.7V differential HCSL outputs: configurable for PCIe (100MHz) and sRIO (125MHz) clock signals
- Selectable crystal oscillator interface, 25MHz, 18pF parallel resonant crystal or LVCMOS/LVTTL single-ended reference clock input
- Supports the following output frequencies: 100MHz or 125MHz
- VCO: 500MHz
- PLL bypass and output enable
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.5ps (typical)
- PCI Express (2.5 Gb/S), Gen 2 (5 Gb/s) and Gen 3 (8 Gb/s) jitter compliant
- Full 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment

| | | | |
|----------|----|----|--------|
| REF_SEL | 1 | 28 | VDDA |
| REF_IN | 2 | 27 | BYPASS |
| VDD | 3 | 26 | IREF |
| GND | 4 | 25 | FSEL |
| XTAL_IN | 5 | 24 | VDD |
| XTAL_OUT | 6 | 23 | nQ3 |
| MR | 7 | 22 | Q3 |
| VDD | 8 | 21 | nQ2 |
| OE3 | 9 | 20 | Q2 |
| OE2 | 10 | 19 | GND |
| OE1 | 11 | 18 | nQ1 |
| OE0 | 12 | 17 | Q1 |
| GND | 13 | 16 | nQ0 |
| VDD | 14 | 15 | Q0 |

ICS841604I-01
28-Lead TSSOP, 240MIL
6.1mm x 9.7mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---------------|--------------------|--------|----------|--|
| 1 | REF_SEL | Input | Pulldown | Reference select. Selects the input reference source. LVCMOS/LVTTL interface levels. See Table 3A. |
| 2 | REF_IN | Input | Pulldown | LVCMOS/LVTTL PLL reference clock input. |
| 3, 8, 14, 24 | V _{DD} | Power | | Core supply pins. |
| 4, 13, 19 | GND | Power | | Power supply ground. |
| 5, 6 | XTAL_IN, XTAL_OUT | Input | | Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. (PLL reference.) |
| 7 | MR | Input | Pulldown | Active HIGH master reset. When logic HIGH, the internal dividers are reset. When logic LOW, the internal dividers are enabled. See Table 3D. LVCMOS/LVTTL interface levels. |
| 9, 10, 11, 12 | OE3, OE2, OE1, OE0 | Input | Pulldown | Output enable pins. LVCMOS/LVTTL interface levels. See Table 3D. |
| 15, 16 | Q0, nQ0 | Output | | Differential output pair. HCSL interface levels. |
| 17, 18 | Q1, nQ1 | Output | | Differential output pair. HCSL interface levels. |
| 20, 21 | Q2, nQ2 | Output | | Differential output pair. HCSL interface levels. |
| 22, 23 | Q3, nQ3 | Output | | Differential output pair. HCSL interface levels. |
| 25 | FSEL | Input | Pulldown | Output frequency select pin. LVCMOS/LVTTL interface levels. See Table 3B. |
| 26 | IREF | Output | | 0.7V current reference resistor output. An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode Qx, nQx clock outputs. |
| 27 | BYPASS | Input | Pulldown | Selects PLL operation/PLL bypass operation. Asynchronous function. LVCMOS/LVTTL interface levels. See Table 3C. |
| 28 | V _{DDA} | Power | | Analog supply pin. |

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |

Function Tables

Table 3A. REF_SEL Function Table

| Input | |
|---------|-----------------|
| REF_SEL | Input Reference |
| 0 | XTAL (default) |
| 1 | REF_IN |

Table 3B. FSEL Function Table ($f_{REF} = 25\text{MHz}$)

| Inputs | | Outputs |
|--------|-----------|-------------------------------|
| FSEL | N Divider | Q[0:3], nQ[0:3] |
| 0 | 5 | VCO/5 (100MHz) PCIe (default) |
| 1 | 4 | VCO/4 (125MHz) sRIO |

Table 3C. BYPASS Function Table

| Input | |
|--------|--|
| BYPASS | PLL Configuration |
| 0 | PLL enabled (default) |
| 1 | PLL bypassed ($f_{OUT} = f_{REF}/N$) |

Table 3D. MR, OEx Function Table

| Inputs | | Outputs |
|----------------|---------|--|
| MR | OE[0:3] | Q[0:3], nQ[0:3] |
| 0 (default) | OE3 = 0 | Q3, nQ3 are High-Impedance (default) |
| | OE3 = 1 | Q3, nQ3 are enabled |
| | OE2 = 0 | Q2, nQ2 are High-Impedance (default) |
| | OE2 = 1 | Q2, nQ2 are enabled |
| | OE1 = 0 | Q1, nQ1 are High-Impedance (default) |
| | OE1 = 1 | Q1, nQ1 are enabled |
| | OE0 = 0 | Q0, nQ0 are High-Impedance (default) |
| | OE0 = 1 | Q0, nQ0 are enabled |
| 1 | X | All outputs are High-Impedance, all internal dividers are reset |

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|--|--|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I XTAL_IN Other Inputs | 0V to V_{DD} -0.5V to $V_{DD} + 0.5V$ |
| Outputs, V_O | -0.5V to $V_{DD} + 0.5V$ |
| Package Thermal Impedance, θ_{JA} | 64.5°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|-----------------|---------|----------|-------|
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | $V_{DD} - 0.20$ | 3.3 | V_{DD} | V |
| I_{DD} | Power Supply Current | OE[0:3] = 0 | | | 87 | mA |
| I_{DDA} | Analog Supply Current | OE[0:3] = 0 | | | 20 | mA |

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|---|--------------------------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | REF_IN, REF_SEL, BYPASS, F_SEL, MR, OE{0:3} | $V_{DD} = V_{IN} = 3.465V$ | | 150 | μA |
| I_{IL} | Input Low Current | REF_IN, REF_SEL, BYPASS, F_SEL, MR, OE{0:3} | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | μA |

Table 5. Crystal Characteristics

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

NOTE: Characterized using an 18pF parallel resonant crystal.

AC Electrical Characteristics

Table 6A. PCI Express Jitter Specifications, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | PCIe Industry Specification | Units |
|--|---|--|---------|---------|---------|-----------------------------|-------|
| t_j (PCIe Gen 1) | Phase Jitter Peak-to-Peak; NOTE 1, 4 | $f = 100\text{MHz}$, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2) | | 12.1 | 28 | 86 | ps |
| | | $f = 125\text{MHz}$, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2) | | 11.7 | 30 | | ps |
| $t_{\text{REFCLK_HF_RMS}}$ (PCIe Gen 2) | Phase Jitter RMS; NOTE 2, 4 | $f = 100\text{MHz}$, 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2) | | 0.82 | 2.15 | 3.1 | ps |
| | | $f = 125\text{MHz}$, 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2) | | 0.8 | 2.2 | | ps |
| $t_{\text{REFCLK_LF_RMS}}$ (PCIe Gen 2) | Phase Jitter RMS; NOTE 2, 4 | $f = 100\text{MHz}$, 25MHz Crystal Input Low Band: 10kHz - 1.5MHz | | 0.15 | 0.47 | 3.0 | ps |
| | | $f = 125\text{MHz}$, 25MHz Crystal Input Low Band: 10kHz - 1.5MHz | | 0.15 | 0.55 | | ps |
| $t_{\text{REFCLK_RMS}}$ (PCIe Gen 3) | Phase Jitter RMS; NOTE 3, 4 | $f = 100\text{MHz}$, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2) | | 0.17 | 0.41 | 0.8 | ps |
| | | $f = 125\text{MHz}$, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2) | | 0.17 | 0.45 | | ps |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the PCI Express Application Note section in the datasheet.

NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 106 clock periods.

NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{\text{REFCLK_HF_RMS}}$ (High Band) and 3.0ps RMS for $t_{\text{REFCLK_LF_RMS}}$ (Low Band).

NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI Express Base Specification Revision 0.7, October 2009 and is subject to change pending the final release version of the specification.

NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

AC Electrical Characteristics

Table 6B. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|---|--------------------------------------|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | VCO/5 | | 100 | | MHz |
| | | VCO/4 | | 125 | | MHz |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 1 | 100MHz (1.875MHz – 20MHz) | | 0.47 | 0.98 | ps |
| | | 125MHz (1.875MHz – 20MHz) | | 0.50 | 1.02 | ps |
| $f_{jit}(cc)$ | Cycle-to-Cycle Jitter; NOTE 2 | | | | 60 | ps |
| $t_{sk}(o)$ | Output Skew; NOTE 2, 3 | | | | 70 | ps |
| V_{MAX} | Absolute Maximum Output Voltage; NOTE 4, 5 | | | | 1150 | mV |
| V_{MIN} | Absolute Minimum Output Voltage; NOTE 4, 6 | | -300 | | | mV |
| V_{RB} | Ringback Voltage; NOTE 7, 8 | | -100 | | 100 | mV |
| t_{STABLE} | Time before V_{RB} is allowed; NOTE 7, 8 | | 500 | | | ps |
| V_{CROSS} | Absolute Crossing Voltage; NOTE 4, 9, 10 | | 220 | | 530 | mV |
| ΔV_{CROSS} | Total Variation of V_{CROSS} ; NOTE 4, 9, 11 | | | | 150 | mV |
| t_{SLEW} | Rising/Falling Edge Rate; NOTE 7, 12 | Measured between -150mV to +150mV | 0.6 | | 4.0 | V/ns |
| odc | Output Duty Cycle; NOTE 7 | | 47 | | 53 | % |
| t_L | PLL Lock Time | | | | 90 | ms |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 5 | ns |
| $t_{PZL, ZH}$ | Output Enable Time | | | | 5 | ns |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Refer to the Phase Noise Plots.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3 Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 4 Measurement taken from a single-ended waveform.

NOTE 5: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 6: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 7: Measurement taken from a differential waveform.

NOTE 8: T_{STABLE} is the time the differential clock must maintain a minimum $\pm 150mV$ differential voltage after rising/falling edges before it is allowed to drop back into the $V_{RB} \pm 100$ differential range. See Parameter Measurement Information Section.

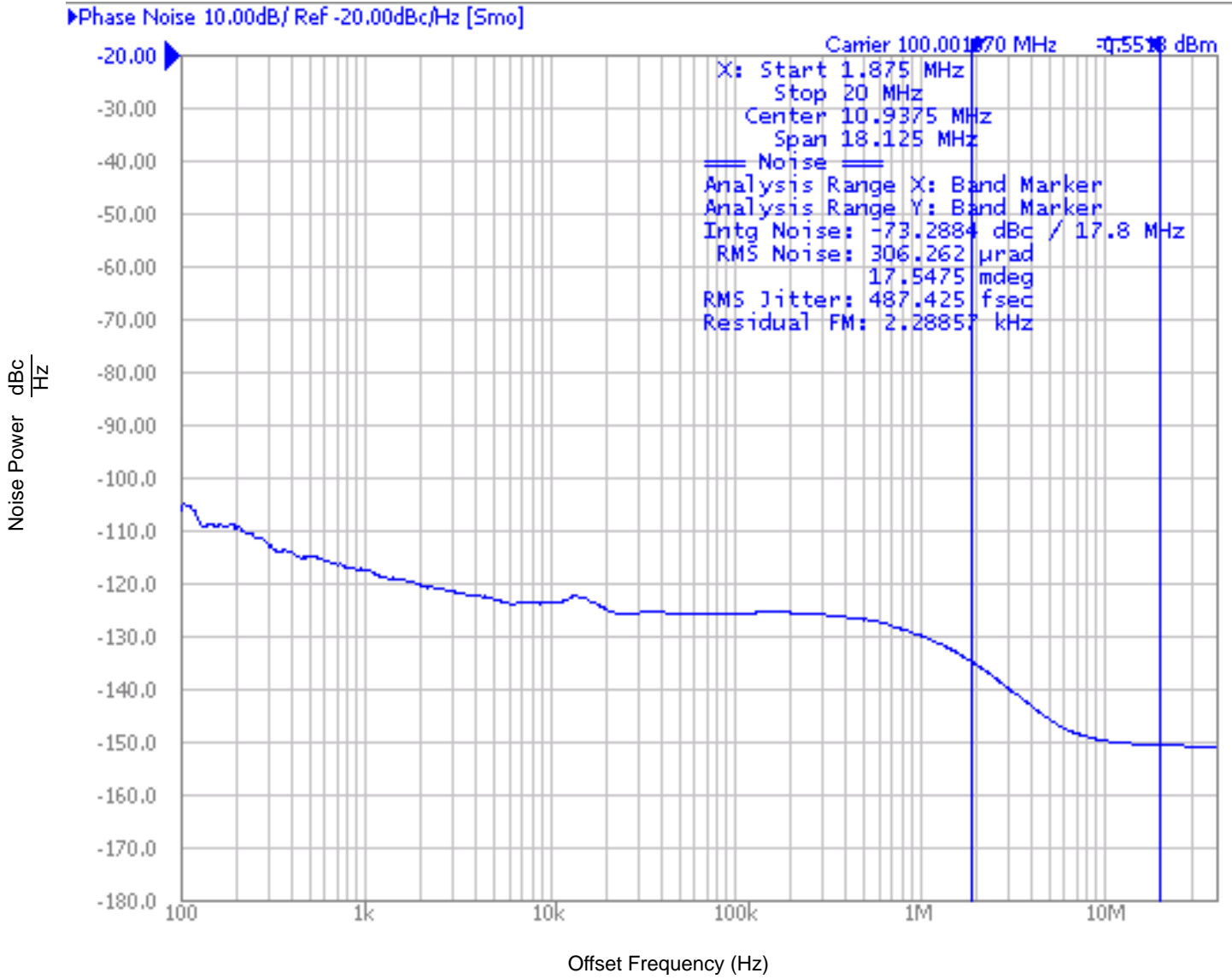
NOTE 9: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx. See Parameter Measurement Information Section.

NOTE 10: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.

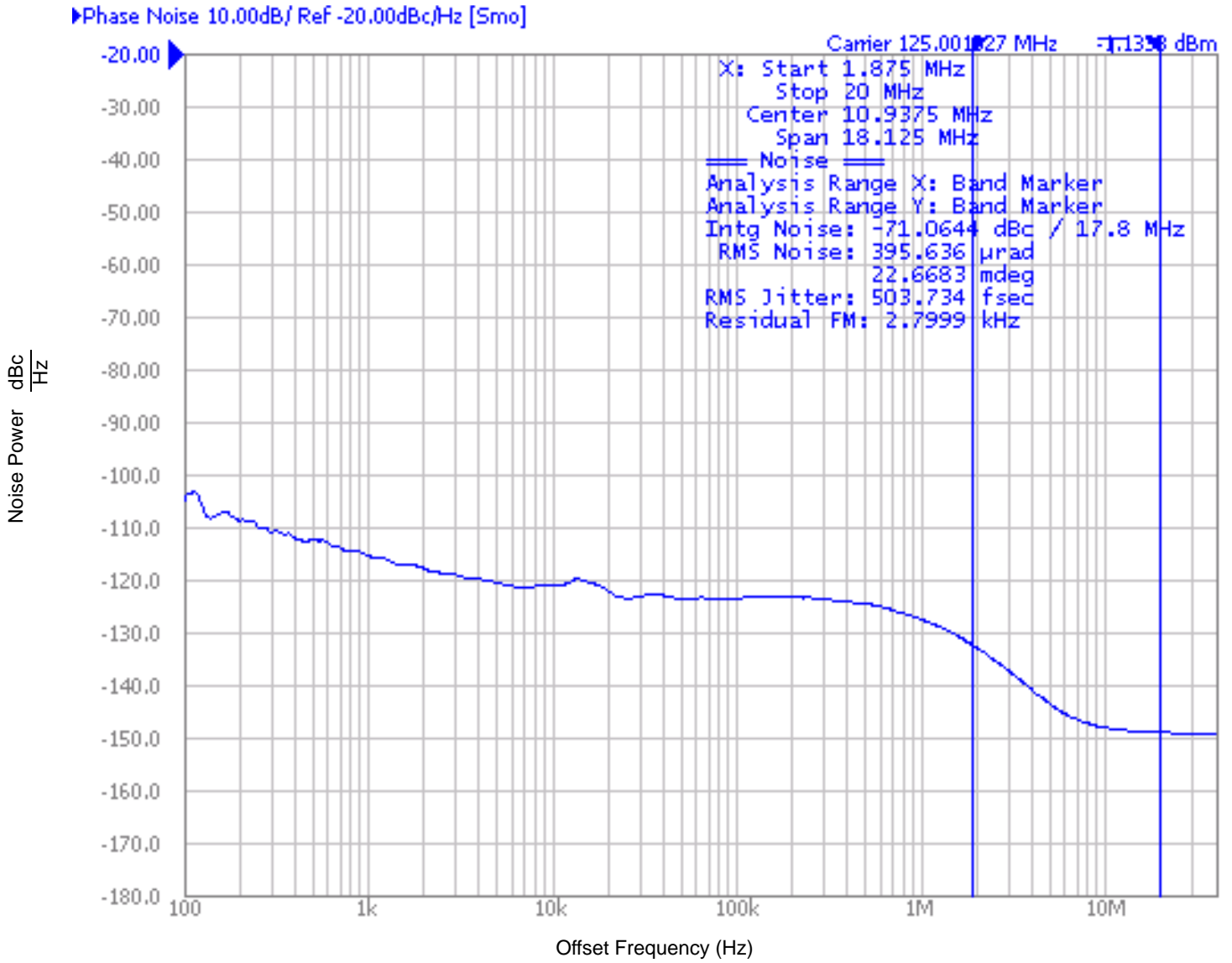
NOTE 11: Defined as the total variation of all crossing voltage of rising Qx and falling nQx. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.

NOTE 12: Measured from -150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Parameter Measurement Information Section.

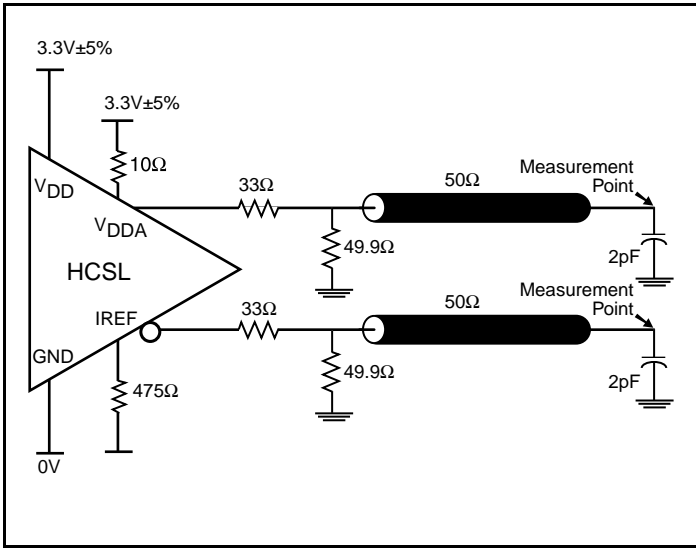
Typical Phase Noise at 100MHz



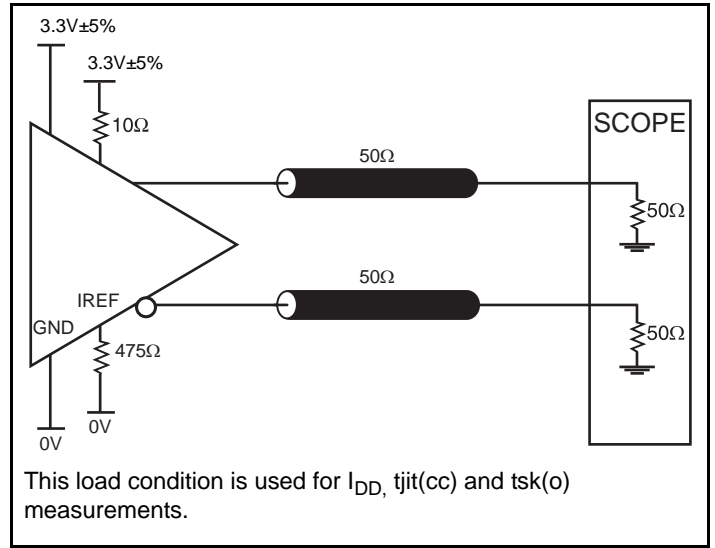
Typical Phase Noise at 125MHz



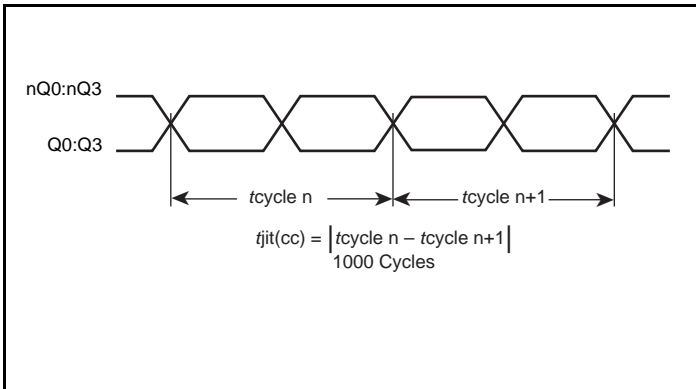
Parameter Measurement Information



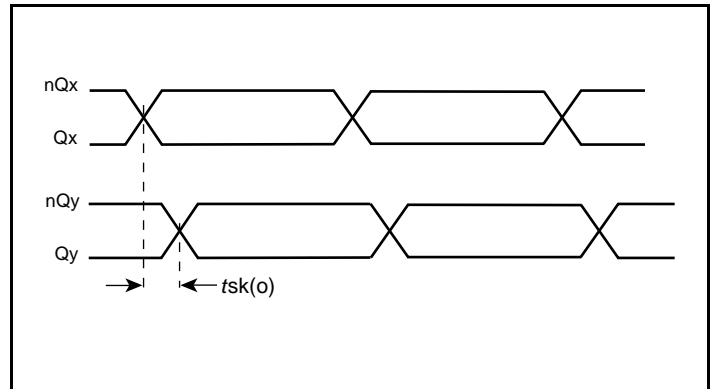
3.3V HCSL Output Load AC Test Circuit



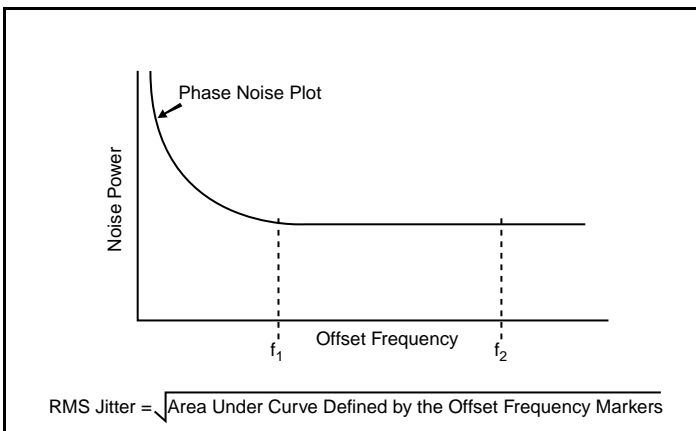
3.3V HCSL Output Load AC Test Circuit



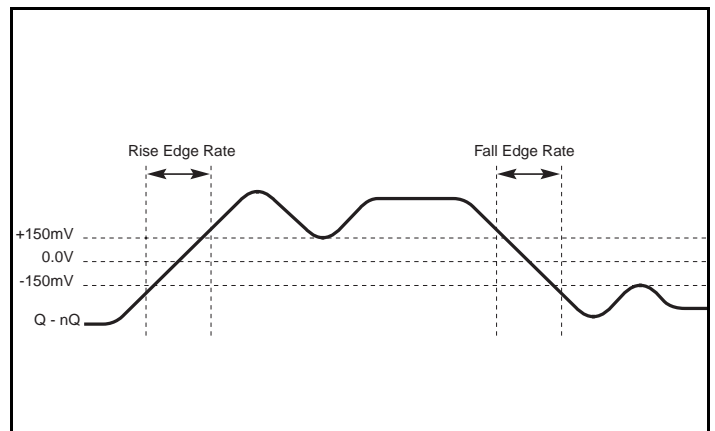
Cycle-to-Cycle Jitter



Output Skew

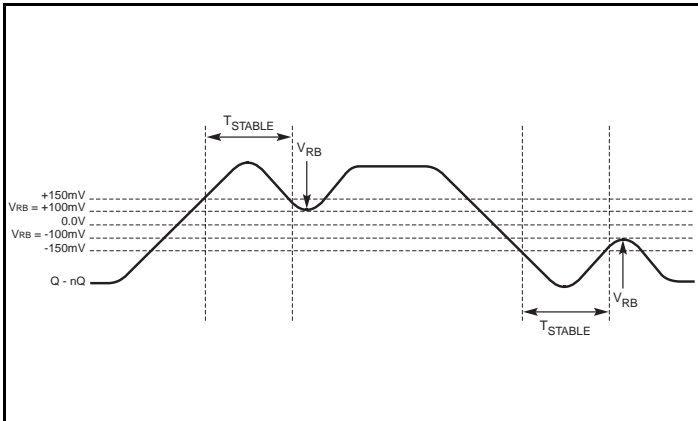


RMS Phase Jitter

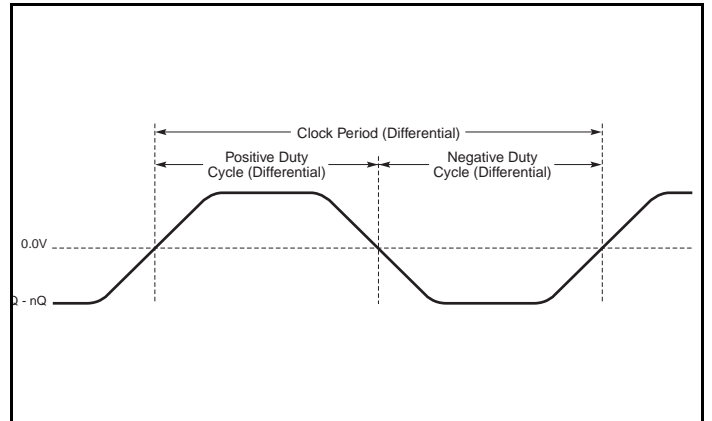


Differential Measurement Points for Rise/Fall Edge Rate

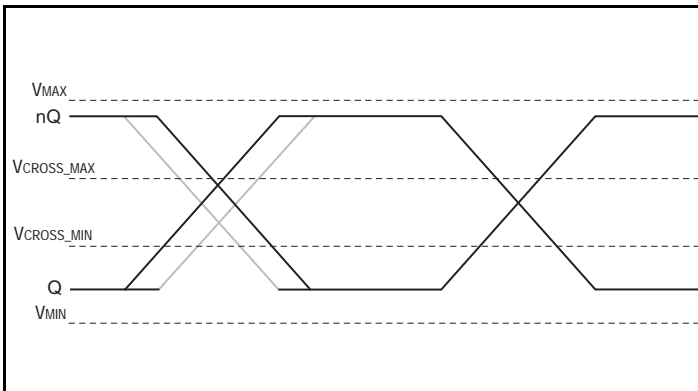
Parameter Measurement Information, continued



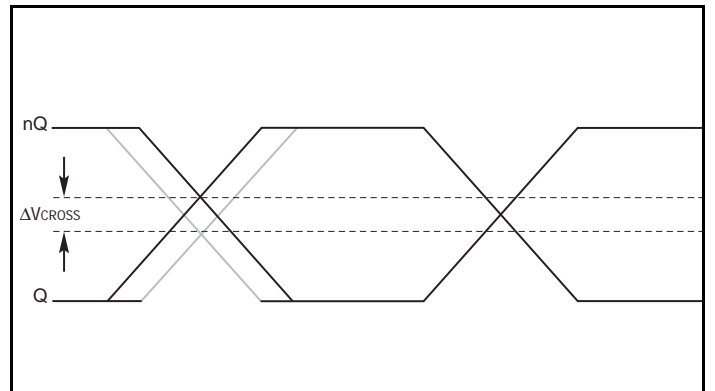
Differential Measurement Points for Ringback



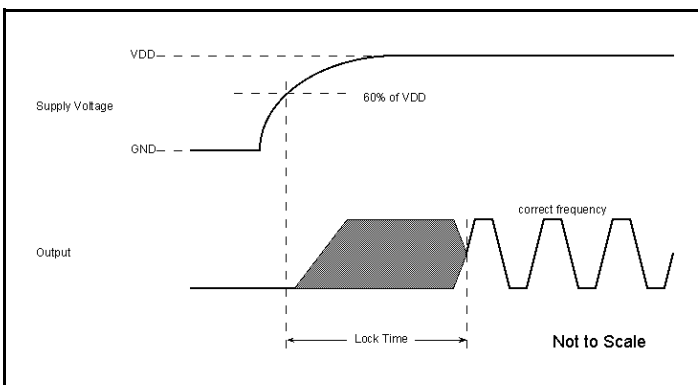
Differential Measurement Points for Duty Cycle/Period



Single-ended Measurement Points for Absolute Cross Point/Swing



Single-ended Measurement Points for Delta Cross Point



PLL Locktime

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

LVC MOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

REF_IN

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_IN to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

Outputs:

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 1A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (R_o) plus the series resistance (R_s) equals the transmission line impedance. In addition,

matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

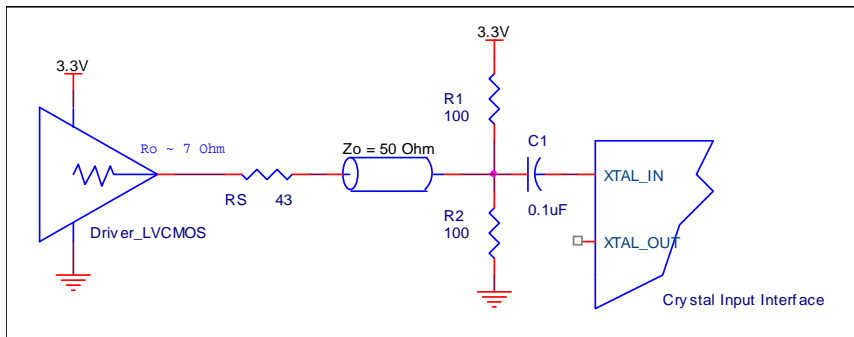


Figure 1A. General Diagram for LVC MOS Driver to XTAL Input Interface

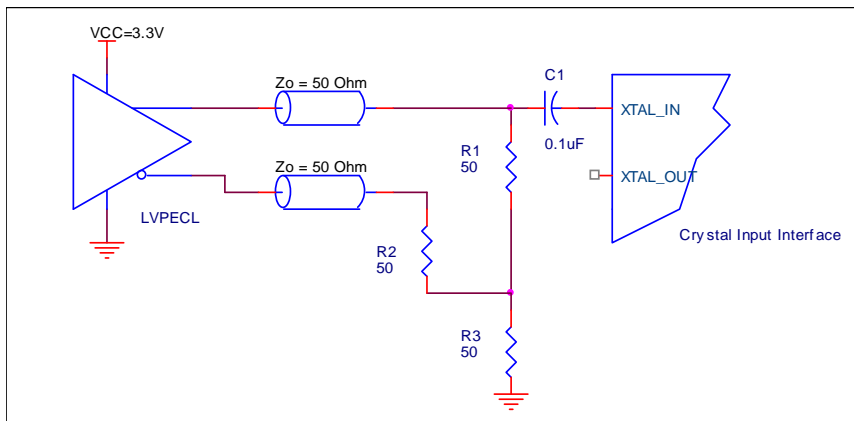


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

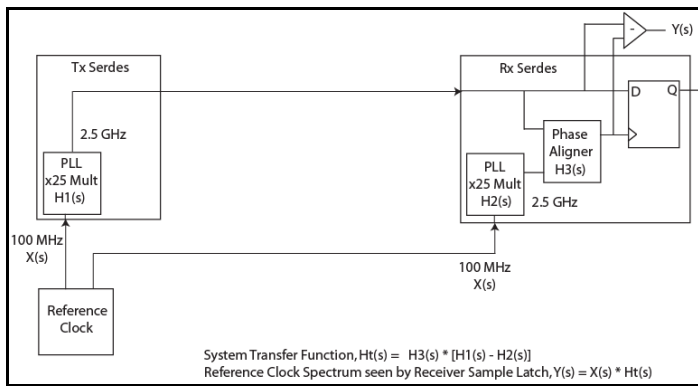
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$H_t(s) = H_3(s) \times [H_1(s) - H_2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

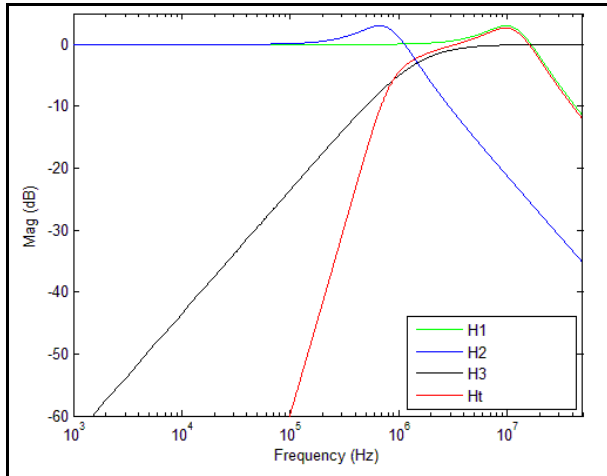
$$Y(s) = X(s) \times H_3(s) \times [H_1(s) - H_2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



PCI Express Common Clock Architecture

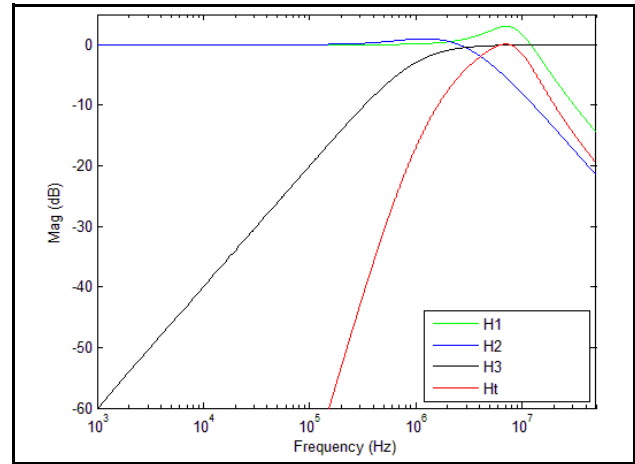
For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g. for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.



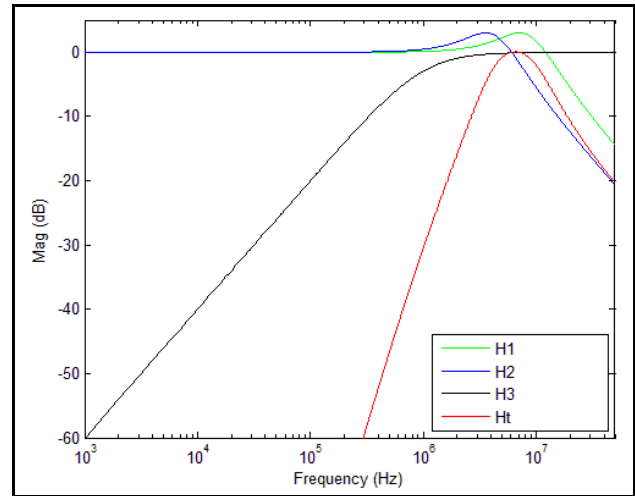
PCI Express Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the

individual transfer functions as well as the overall transfer function Ht.

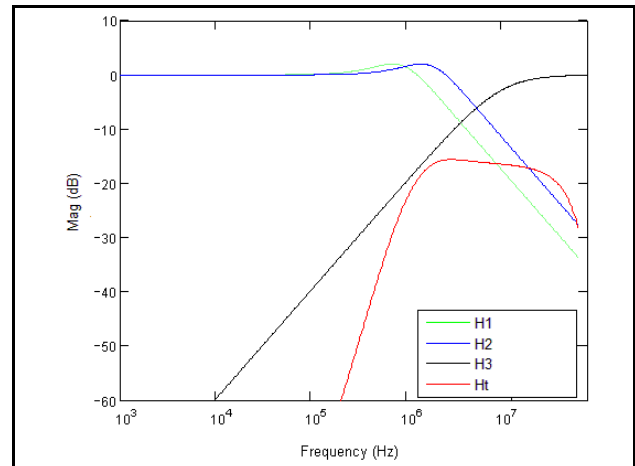


PCI Express Gen 2A Magnitude of Transfer Function



PCI Express Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCI Express Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements*.

Recommended Termination

Figure 2A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output

types. All traces should be 50Ω impedance single-ended or 100Ω differential.

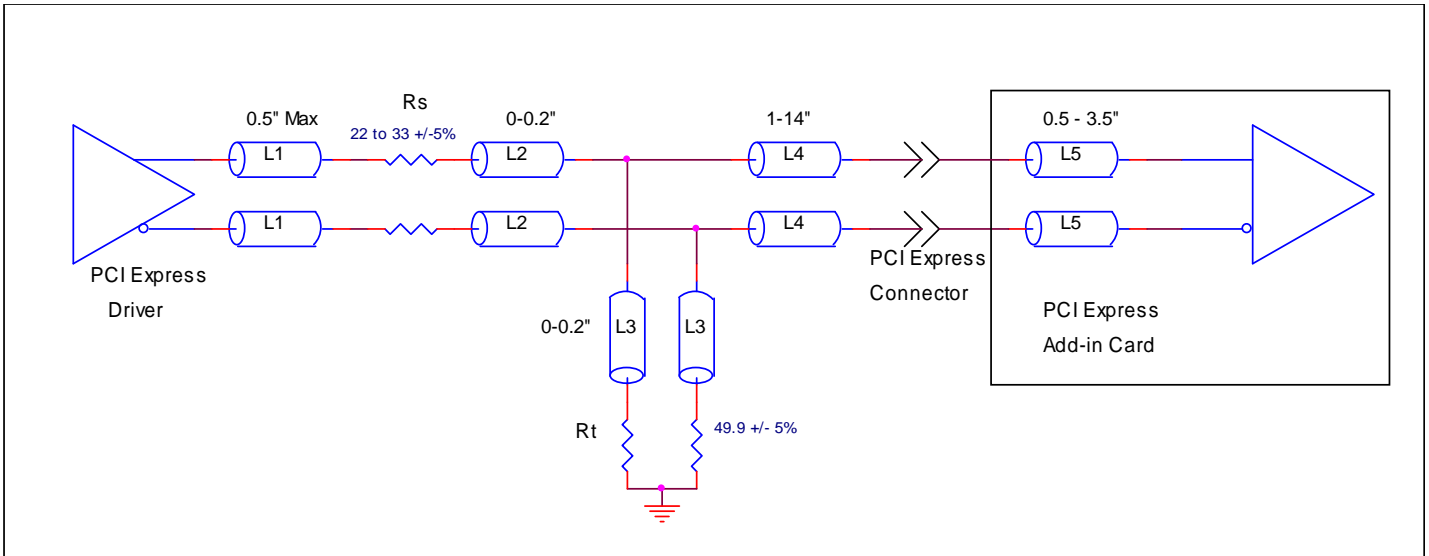


Figure 2A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 2B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will

be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

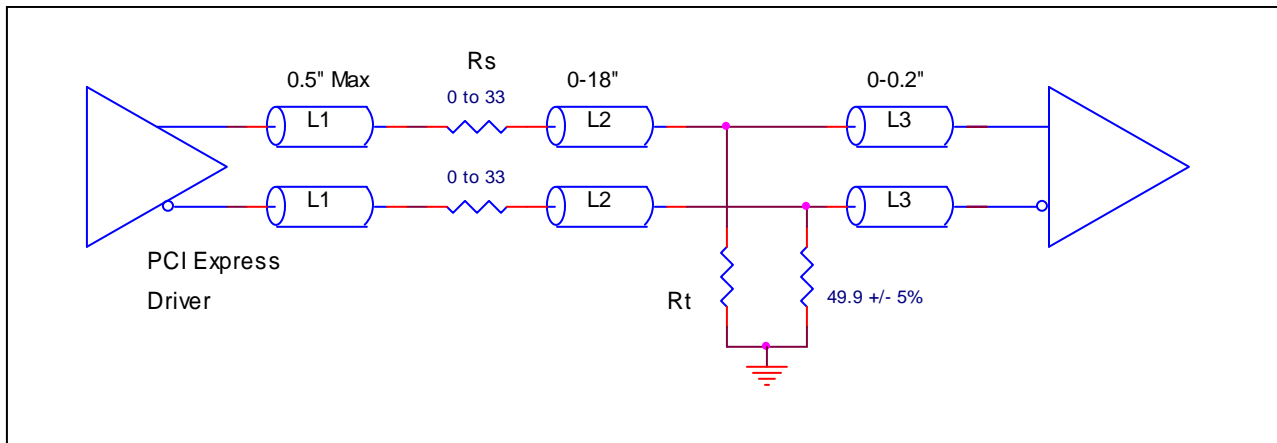


Figure 2B. Recommended Termination (where a point-to-point connection can be used)

Schematic Example

Figure 3 shows an example of ICS841604I-01 application schematic. In this example, the device is operated at $V_{DD} = 3.3V$. The 18pF parallel resonant 25MHz crystal is used. The load capacitance $C1 = 27pF$ and $C2 = 27pF$ are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting $C1$ and $C2$. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS841604I-01 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power

pins as possible. If space is limited, the 0.1uf capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB. Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

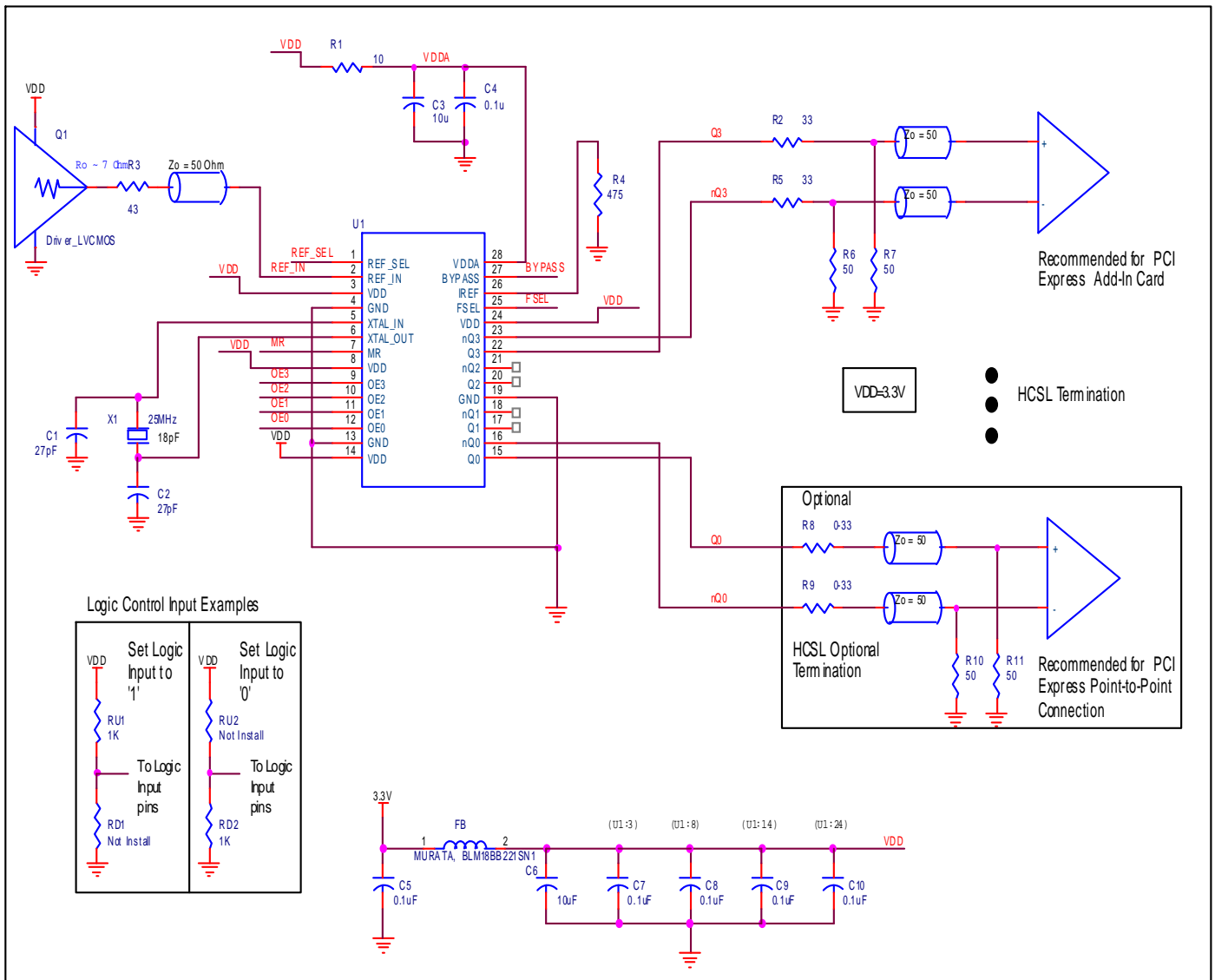


Figure 3. ICS841604I-01 Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS841604I-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS841604I-01 is the sum of the core power plus analog plus the power dissipation in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (87mA + 20mA) = \mathbf{370.755mW}$
- Power (outputs)_{MAX} = **44.5mW/Loaded Output pair**
Power (output)_{MAX} = $44.5mW * 4 = \mathbf{178mW}$

Total Power_{MAX} = (3.465V, with all outputs switching) = $370.755mW + 178mW = \mathbf{548.755mW}$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_{total} + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 64.5°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.549\text{W} * 64.5^\circ\text{C/W} = 120.4^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 28 Lead TSSOP, Forced Convection

| θ_{JA} vs. Air Flow | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 64.5°C/W | 60.4°C/W | 58.5°C/W |

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 4*.

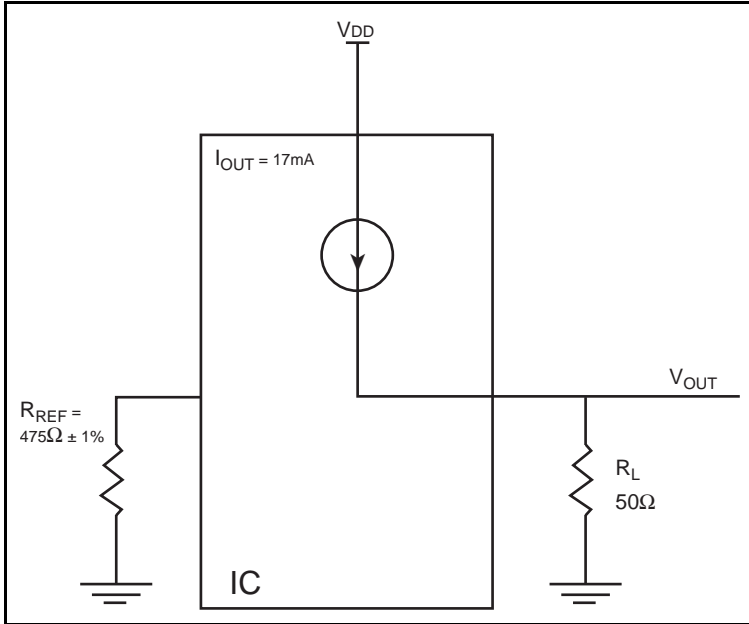


Figure 4. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD_MAX} .

$$\begin{aligned}
 \text{Power} &= (V_{DD_MAX} - V_{OUT}) * I_{OUT}, \\
 \text{since } V_{OUT} &= I_{OUT} * R_L \\
 &= (V_{DD_MAX} - I_{OUT} * R_L) * I_{OUT} \\
 &= (3.465V - 17mA * 50\Omega) * 17mA
 \end{aligned}$$

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 28 Lead TSSOP

| θ_{JA} vs. Air Flow | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 64.5°C/W | 60.4°C/W | 58.5°C/W |

Transistor Count

The transistor count for ICS841604I-01 is: 2760

Package Outline and Package Dimensions

Package Outline - G Suffix for 28 Lead TSSOP

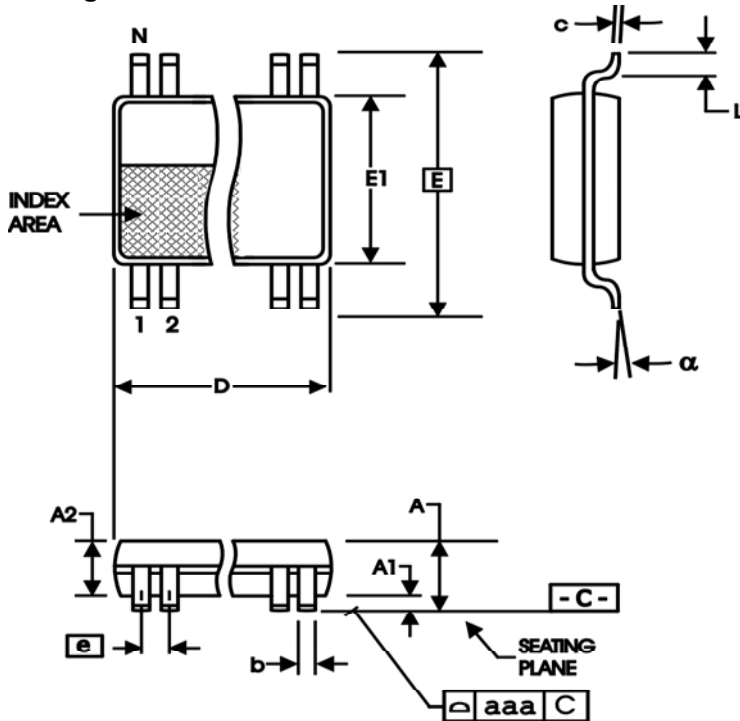


Table 9. Package Dimensions

| All Dimensions in Millimeters | | |
|-------------------------------|------------|---------|
| Symbol | Minimum | Maximum |
| N | 28 | |
| A | | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 9.60 | 9.80 |
| E | 8.10 Basic | |
| E1 | 6.00 | 6.20 |
| e | 0.65 Basic | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|-----------------|---------------------------|--------------------|---------------|
| 841604AGI-01LF | ICS841604AGI01L | "Lead-Free" 28 Lead TSSOP | Tube | -40°C to 85°C |
| 841604AGI-01LFT | ICS841604AGI01L | "Lead-Free" 28 Lead TSSOP | 1000 Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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