2:1, Differential-to-3.3V Dual LVPECL/ECL Clock Multiplexer

85356

DATA SHEET

General Description

The 85356 is a dual 2:1 Differential-to-LVPECL Multiplexer. The device has both common select and individual select inputs. When COM_SEL is logic High, the CLKxx input pairs will be passed to the output. When COM_SEL is logic Low, the output is determined by the setting of the SEL0 pin for channel 0 and the SEL1 pin for Channel 1.

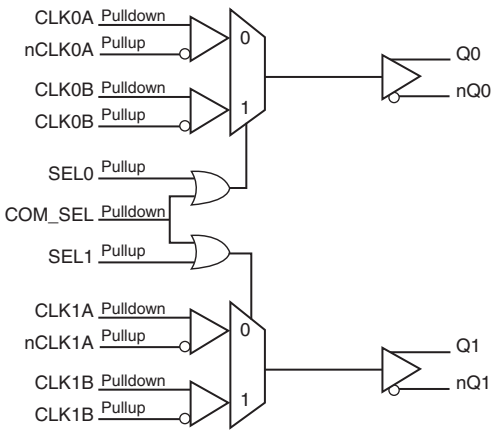
The differential input has a common mode range that can accept most differential input types such as LVPECL, LVDS, LVHSTL, SSTL, and HCSL. The 85356 can therefore be used as a differential translator to translate almost any differential input type to LVPECL. It can also be used in ECL mode by setting V_{CC} = 0V and V_{EE} to -3.0V to - 3.8V.

The 85356 adds negligible jitter to the input clock and can operate at high frequencies in excess of 900MHz thus making it ideal for use in demanding applications such as SONET, Fibre Channel, 1 Gigabit/10 Gigabit Ethernet.

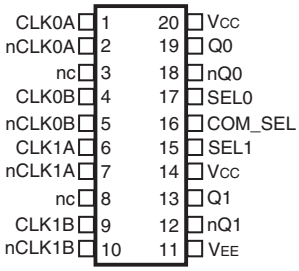
Features

- High speed differential muliplexer. The device can be configured as a 2:1 multiplexer
- Dual 3.3V LVPECL outputs
- Selectable differential CLKx/nCLKx input pairs
- Differential CLKx/nCLKx pairs can accept the following interface levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Output frequency: 900MHz (typical)
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nCLKx input
- Output skew: 75ps (typical)
- Propagation delay: 1.15ns (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 3V to 3.8V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3V to -3.8V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



85356

20-Lead SOIC
7.5mm x 12.8mm x 2.3mm package body
M Package
Top View

85356

20-Lead TSSOP
6.5mm x 4.4mm x 0.92mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
14, 20	V_{CC}	Power		Positive supply pins.
1	CLK0A	Input	Pulldown	Non-inverting differential clock input.
2	nCLK0A	Input	Pullup	Inverting differential clock input.
3, 8	nc	Unused		No connect.
4	CLK0B	Input	Pulldown	Non-inverting differential clock input.
5	nCLK0B	Input	Pullup	Inverting differential clock input.
6	CLK1A	Input	Pulldown	Non-inverting differential clock input.
7	nCLK1A	Input	Pullup	Inverting differential clock input.
9	CLK1B	Input	Pulldown	Non-inverting differential clock input.
10	nCLK1B	Input	Pullup	Inverting differential clock input.
11	V_{EE}	Power		Negative supply pin.
12, 13	nQ1,Q1	Output		Differential output pair. LVPECL interface levels.
15, 17	SEL1, SEL0	Input	Pullup	Clock select inputs. LVCMOS/LVTTL interface levels.
16	COM_SEL	Input	Pulldown	Common select input. LVCMOS/LVTTL interface levels.
18, 19	nQ0,Q0	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3. Control Input Function Table

	Inputs		Outputs			
COM_SEL	SEL1	SEL0	Q0	nQ0	Q1	nQ1
0	0	0	CLK0A	nCLK0A	CLK1A	nCLK1A
0	0	1	CLK0B	nCLK0B	CLK1A	nCLK1A
0	1	0	CLK0A	nCLK0A	CLK1B	nCLK1B
0	1	1	CLK0B	nCLK0B	CLK1B	nCLK1B
1	x	x	CLK0B	nCLK0B	CLK1B	nCLK1B

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC}+ 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA} 20 Lead SOIC 20 Lead TSSOP	 46.2°C/W (0 lfpm) 73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V±0.3V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.0	3.3	3.6	V
I_{EE}	Power Supply Current				40	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V±0.3V; V_{EE} = 0V, T_A = -40°C to 85°**C**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	SEL0, SEL1	V_{CC} = V_{IN} = 3.6V			5	µA
		COM_SEL	V_{CC} = V_{IN} = 3.6V			150	µ
I_{IL}	Input Low Current	SEL0, SEL1	V_{CC} = 3.6V, V_{IN} = 0V	-150			µA
		COM_SEL	V_{CC} = 3.6V, V_{IN} = 0V	-5			µ

Table 4C. Differential DC Characteristics, V_{CC} = 3.3V±0.3V; V_{EE} = 0V, T_A = -40°C to 85°**C**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0A, CLK0B, CLK1A, CLK1B	V_{CC} = V_{IN} = 3.6V			150	µA
		nCLK0A, nCLK0B, nCLK1A, nCLK1B	V_{CC} = V_{IN} = 3.6V			5	µA
I_{IL}	Input Low Current	CLK0A, CLK0B, CLK1A, CLK1B	V_{CC} = 3.6V, V_{IN} = 0V	-5			µA
		nCLK0A, nCLK0B, nCLK1A, nCLK1B	V_{CC} = 3.6V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.0	V
V_{CMR}	Common Mode Range; NOTE 1, 2			V_{EE} + 0.5		V_{CC} – 0.85	V

NOTE 1: VIL should not be less than -0.3V
NOTE 2: Common mode voltage is defined as V_{IH}.

Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V±0.3V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{CC} – 2V.

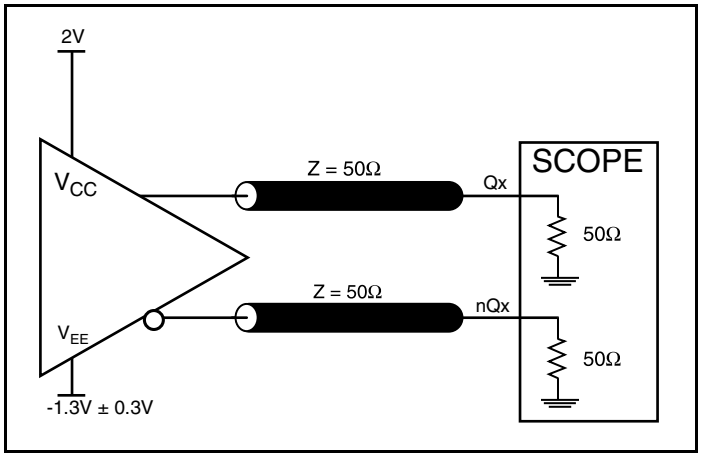
AC Electrical Characteristics

Table 5. AC Characteristics, V_{CC} = 3.3V±0.3V; V_{EE} = 0V, T_A = -40°C to 85°C

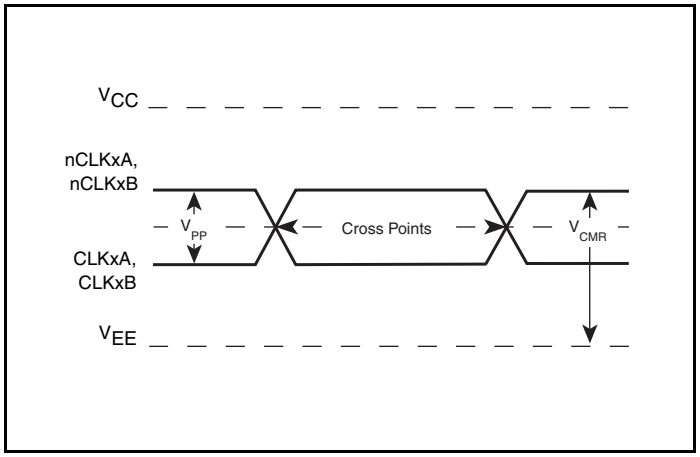
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			900		MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 900MHz	0.85	1.15	1.45	ns
$t$sk(o)	Output Skew; NOTE 2, 3			75	150	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		580	ps
t_{ODC}	Output Duty Cycle Skew				100	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions
NOTE: All parameters measured at $f \leq$ 622MHz, unless otherwise noted.
NOTE: This part does not add measurable jitter.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: This parameter is defined according with JEDEC Standard 65.

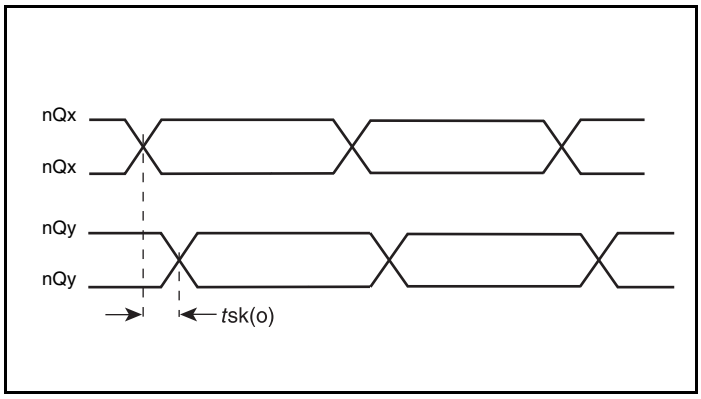
Parameter Measurement Information



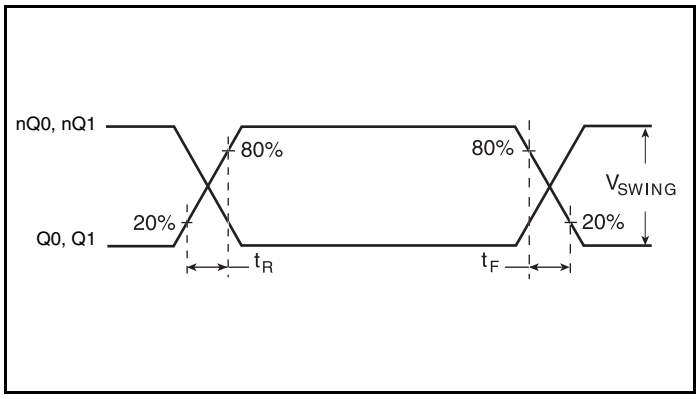
LVPECL Output Load AC Test Circuit



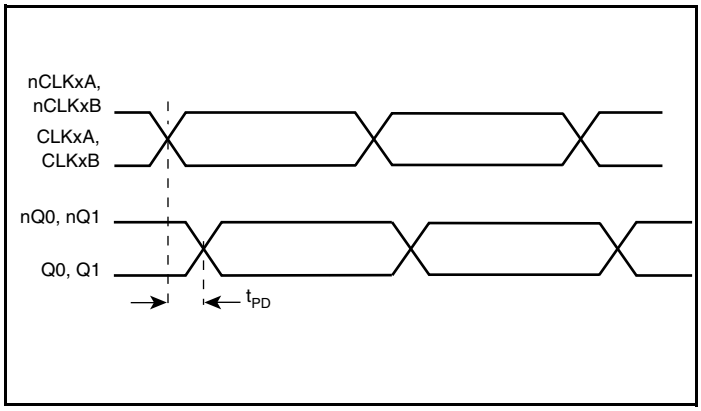
Differential Input Level



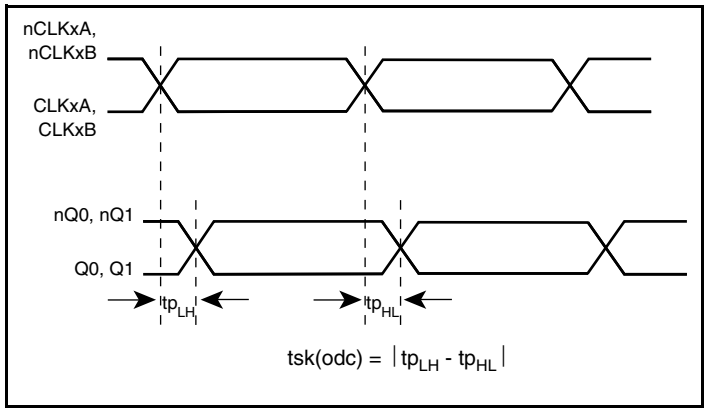
Output Skew



Output Rise/Fall Time



Propagation Delay



Output Duty Cycle Skew

Application Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

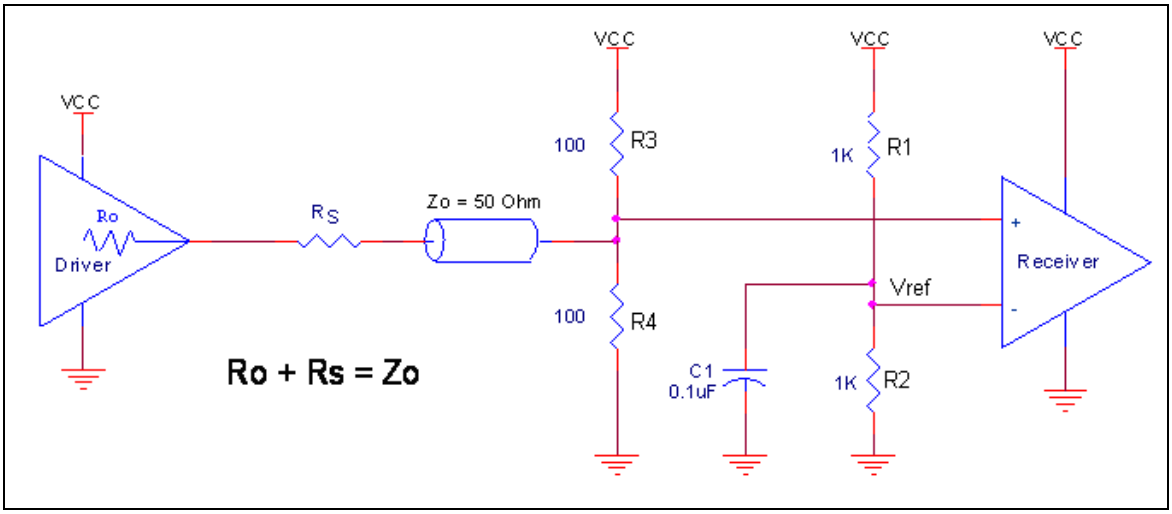


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Inputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

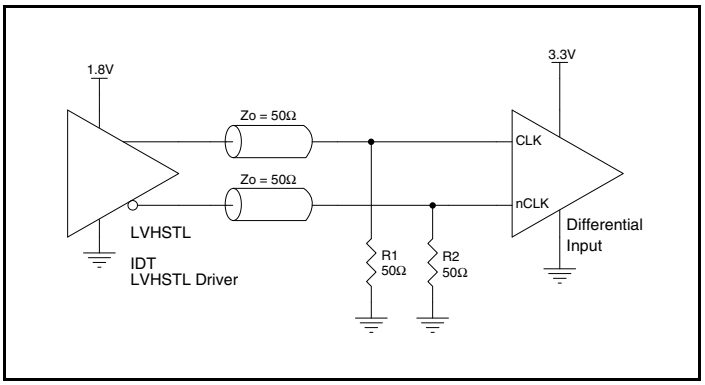


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

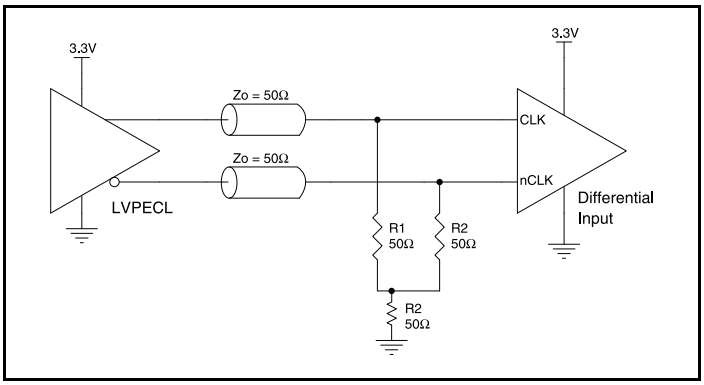


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

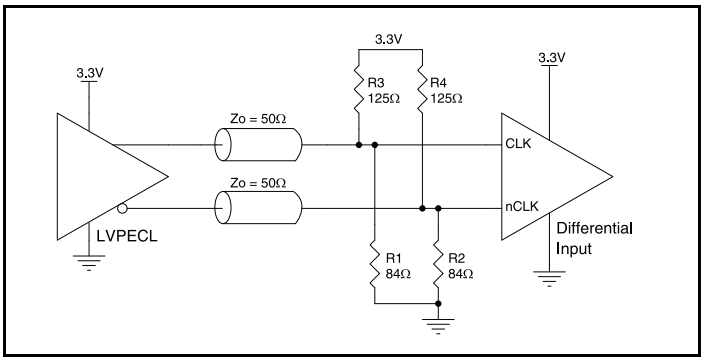


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

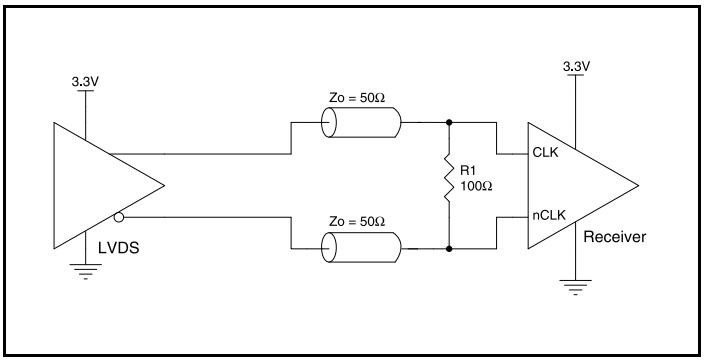


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

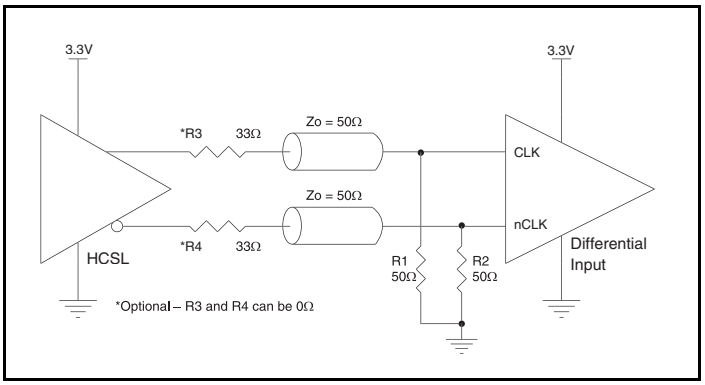


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

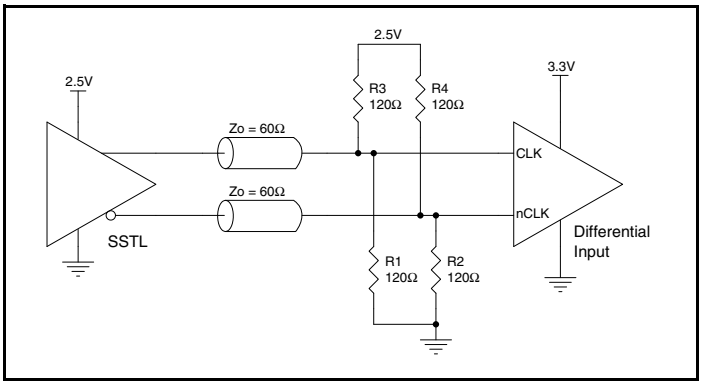


Figure 2F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

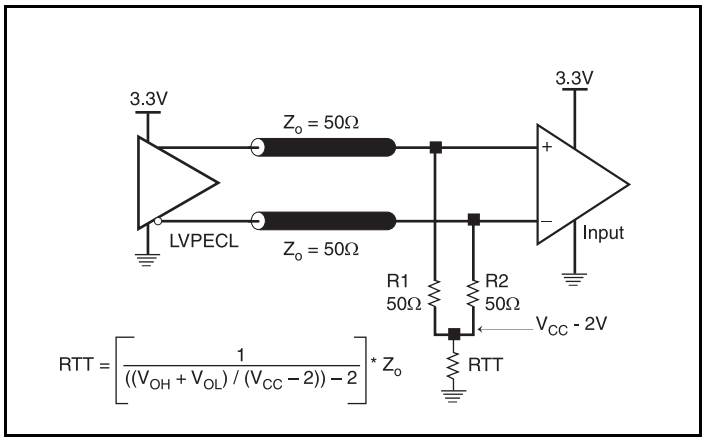


Figure 3A. 3.3V LVPECL Output Termination

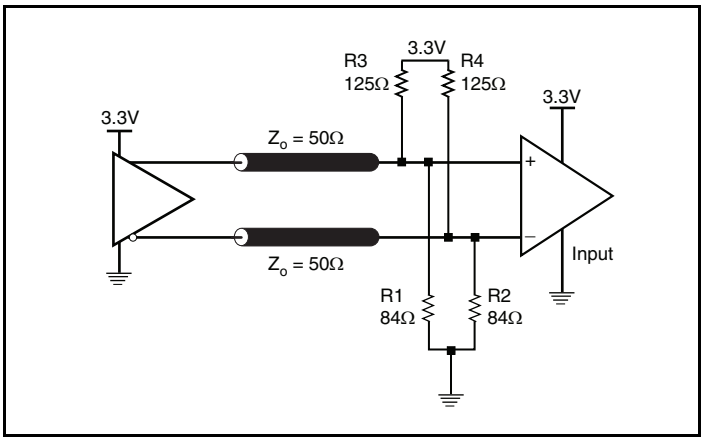


Figure 3B. 3.3V LVPECL Output Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the 85356.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 85356 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 0.3V = 3.6V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.6V * 40mA = **144mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power$_{\_MAX}$ (3.6V, with all outputs switching) = 144mW + 60mW = **204mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 83.2°C/W per Table 6B below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.204W * 73.2°C/W = 99.9°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6A. Thermal Resistance θ_{JA} for 20 Lead SOIC, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

Table 6B. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 4.*

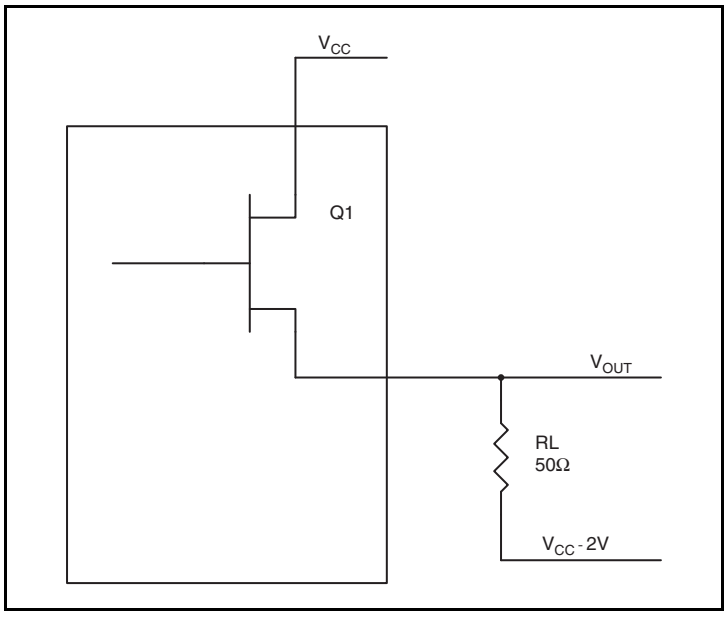


Figure 4. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.9V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 7A. θ_{JA} vs. Air Flow Table for a 20 Lead SOIC, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

Table 7B. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

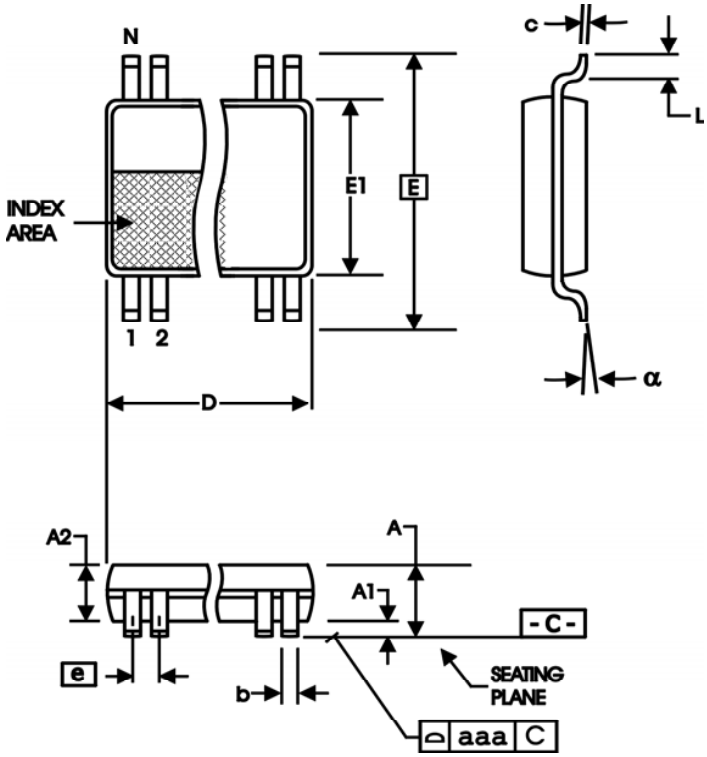
NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 85356 is: 446

Package Outlines and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP



Package Outline - M Suffix for 20 Lead SOIC

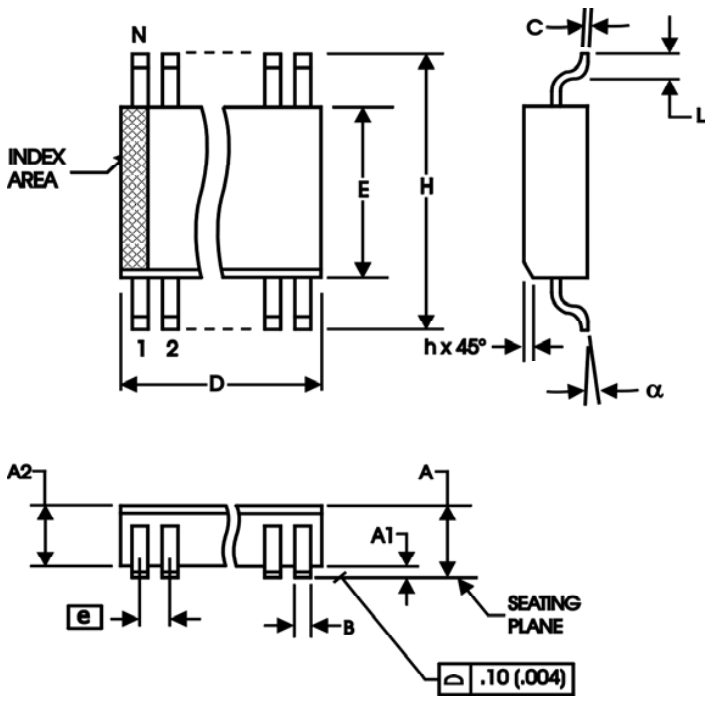


Table 7A. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Table 7B. Package Dimensions for 20 Lead SOIC

300 Millimeters All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		2.65
A1	0.10	
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 Basic	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	7°

Reference Document: JEDEC Publication 95, MS-013, MS-119

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
85356AMILF	85356AMILF	“Lead-Free” 20 Lead SOIC	Tube	-40°C to 85°C
85356AMILFT	85356AMILF	“Lead-Free” 20 Lead SOIC	Tape & Reel	-40°C to 85°C
85356AGILF	ICS85356AGIL	“Lead-Free” 20 Lead TSSOP	Tube	-40°C to 85°C
85356AGILFT	ICS85356AGIL	“Lead-Free” 20 Lead TSSOP	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		7 13	Added Differential Clock Input Interface section. Ordering Information Table - added Lead Free part number. Updated data sheet format.	10/7/04
B	T2 T4D T9	2 4 8-9 13	Pin Characteristics Table - changed C_{IN} 4pF max, to 4pF typical. LVPECL DC Characteristics Table - corrected V_{OH} max. from V_{CC} - 1.0V to V_{CC} - 0.9V. Power Considerations - corrected power dissipation to reflect V_{OH} max in Table 4D. Ordering Information Table - added ICS85356AMI lead-free part/order number and lead-free note.	4/11/07
B		3 5 6 7 9	Absolute Maximum Ratings - added TSSOP Package Thermal Impedance. Parameter Measurement Information - corrected *Output Duty Cycle Skew diagram.* Added *Recommendations for Unused Input/Output Pins* section. Updated *Differential Clock Input Interface* section. Power Considerations - updated Junction Temperature calculation to worst case ambient temperature. Updated datasheet format.	2/14/08
B	T1 T5 T8	2 4 6 8 13	Pin Description Table - corrected nCLKx and SELx pins from Pulldown to Pullup. Made error when converting the datasheet format. AC Characteristics Table - added thermal note. Updated *Wiring the Differential Input to Accept Single-ended Levels.* Updated Figures 3A and 3B. Ordering Information Table - deleted “ICS” prefix for Part/Order column. Added LF marking for SOIC, deleted “ICS” from marking for non-LF SOIC. Updated Header/Footer of datasheet.	5/10/10
C	 T8	1 13	Features section - removed reference to leaded devices Ordering Information - removed leaded devices. PDN CQ-13-02 last time buy expired.	1/5/15

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