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Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

THIS SPEC IS OBSOLETE

Spec No: 001-53516

Spec Title: CY8C20111/CY8C20121, CAPSENSE(R) EXPRESS(TM) - ONE BUTTON AND TWO BUTTON CAPACITIVE CONTROLLERS

Replaced by: NONE

CY8C20111/CY8C20121

CapSense® Express™ – One Button and Two Button Capacitive Controllers

OBSOLETE

Features

- Capacitive button input tied to a configurable output
  - Robust sensing algorithm
  - High sensitivity, low noise
  - Immunity to RF and AC noise
  - Low radiated EMC noise
  - Supports wide range of input capacitance, sensor shapes, and sizes
- Target Applications
  - Printers
  - Cellular handsets
  - LCD monitors
  - Portable DVD players
- Industry's best configurability
  - Custom sensor tuning
  - Output supports strong 20 mA sink current
  - Output state can be controlled through I^2C or directly from CapSense input state
  - Run time reconfigurable over I^2C
- Advanced features
  - Plug-and-play with factory defaults – tuned to support up to 1 mm overlay
  - Nonvolatile storage of custom settings
  - Easy integration into existing products – configure output to match system
  - No external components required
  - World class free configuration tool
- Wide range of operating voltages
  - 2.45 V to 2.9 V
  - 3.10 V to 3.6 V
  - 4.75 V to 5.25 V
- I^2C communication
  - Supported from 1.8 V
  - Internal pull-up resistor support option
  - Data rate up to 400 kbps.
  - Configurable I^2C addressing
- Industrial temperature range: –40 °C to +85 °C
- Available in 8-pin SOIC package

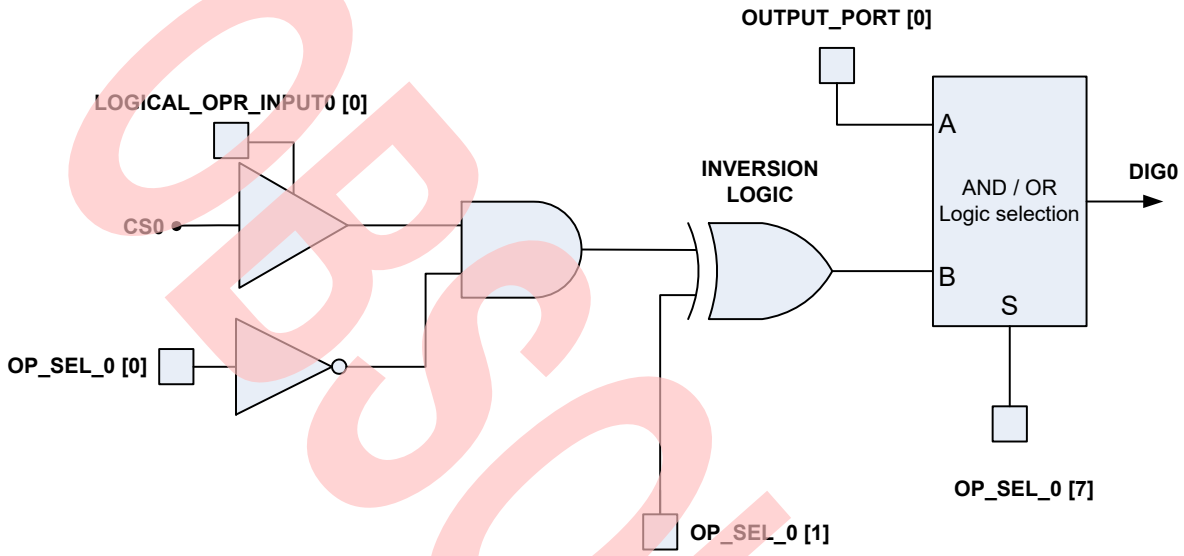
Overview

The CapSense® Express™ controllers support two capacitive sensing (CapSense) buttons and two general purpose outputs in CY8C20121 and one CapSense button and one general purpose output in CY8C20111. The device functionality is configured through the I^2C port and can be stored in on-board nonvolatile memory for automatic loading at power on. The digital outputs are controlled from CapSense inputs in factory default settings, but are user configurable for direct control through I^2C.

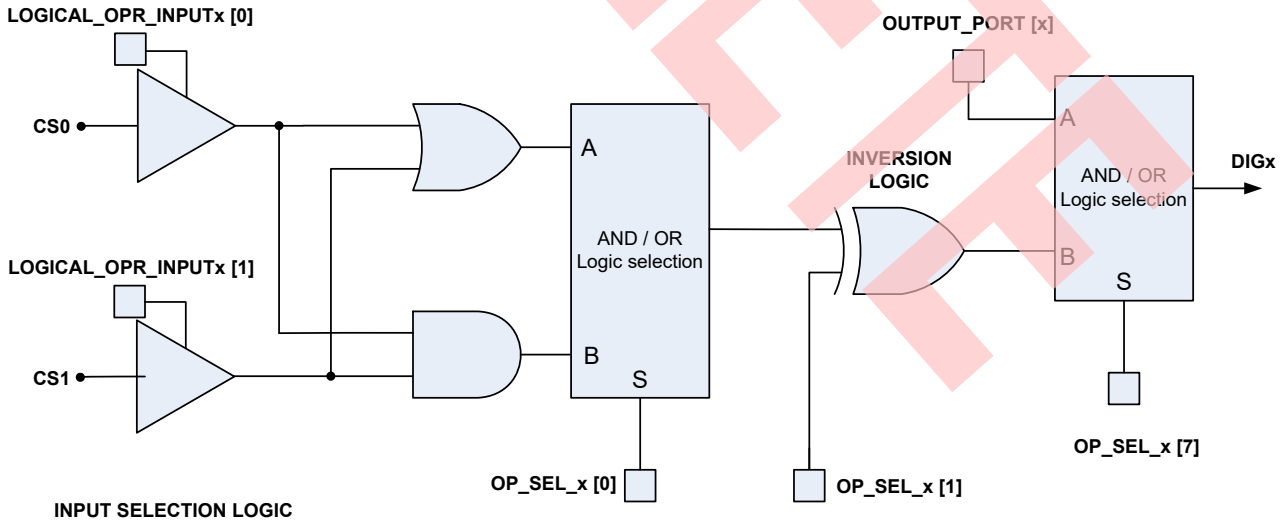
The four key blocks that make up the CY8C20111 and CY8C20121 controllers are: a robust capacitive sensing core with high immunity against radiated and conductive noise, control registers with nonvolatile storage, configurable outputs, and I^2C communications. The user can configure registers with parameters needed to adjust the operation and sensitivity of the CapSense buttons and outputs and permanently store the settings. The standard I^2C serial communication interface allows the host to configure the device and read sensor information in real time. I^2C address is fully configurable without any external hardware strapping.

Errata: For information on silicon errata, see "Errata" on page 41. Details include trigger conditions, devices affected, and proposed workaround.

CY8C20111 Digital Logic Diagram



CY8C20121 Digital Logic Diagram



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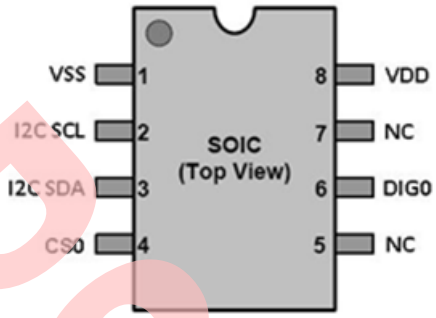
Pinouts

Figure 1. 8-pin SOIC (150 Mils) pinout
CY8C20111 (1 Button)



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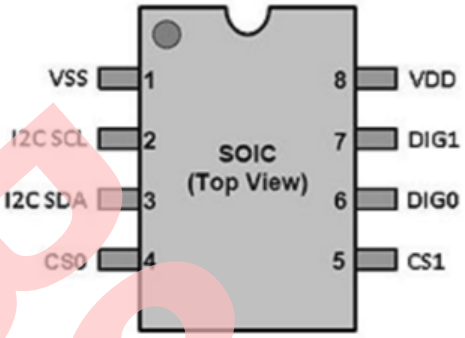
Pin Definitions

8-pin SOIC
CY8C20111 (1 Button)

Pin No	Name	Description
1	V_{SS}	Ground
2	I2C SCL	I^2C Clock
3	I2C SDA	I^2C Data
4	CS0	CapSense Input
5	NC	No Connect
6	DIG0	Digital Output
7	NC	No Connect
8	V_{DD}	Supply Voltage

Pinouts

Figure 2. 8-pin SOIC (150 Mils) pinout
CY8C20121 (2 Button)



Pin Definitions

8-pin SOIC
CY8C20121 (2 Button)

Pin No	Name	Description
1	V_{SS}	Ground
2	I2C SCL	I^2C Clock
3	I2C SDA	I^2C Data
4	CS0	CapSense Input
5	CS1	CapSense Input
6	DIG0	Digital Output
7	DIG1	Digital Output
8	V_{DD}	Supply Voltage

OBSOLETE

Typical Circuits

Figure 3. Circuit-1: One Button and One LED[1]

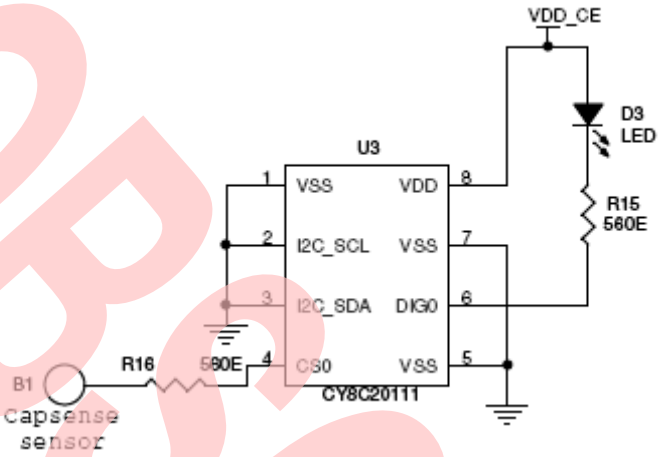
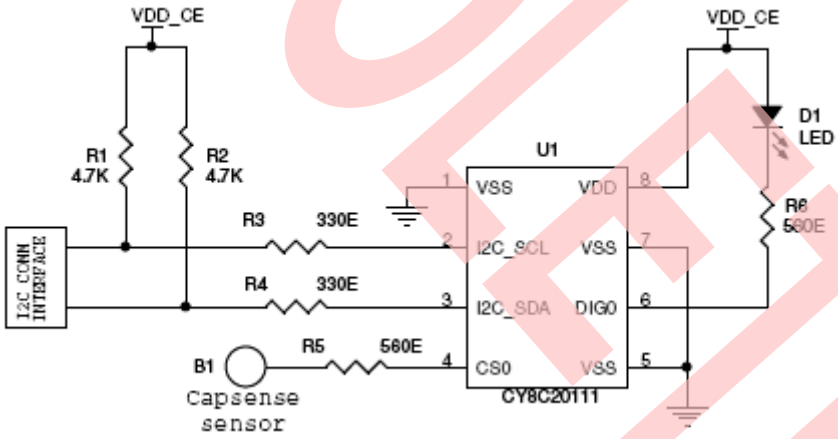


Figure 4. Circuit-2: One Button and One LED with I²C Interface



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Note
1. The sensors are factory tuned to work with 1 mm plastic or glass overlay.

Typical Circuits *(continued)*

Figure 5. Circuit-3: Two Buttons and Two LEDs with I²C Interface

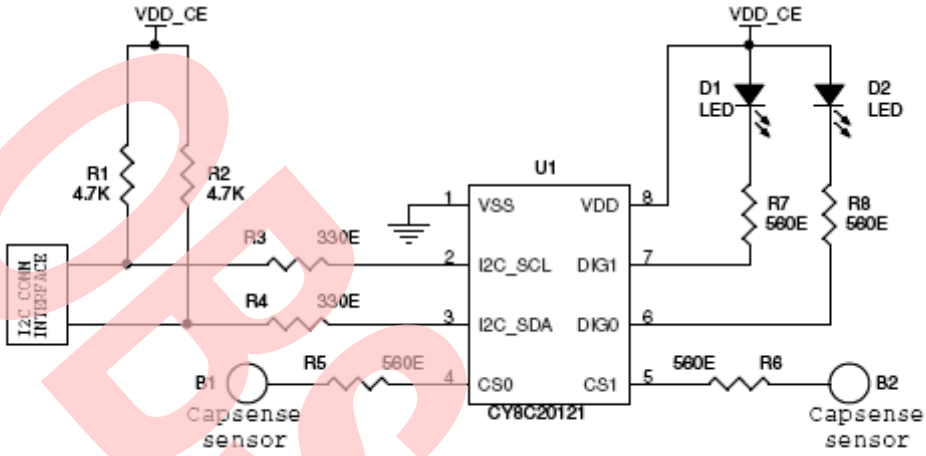
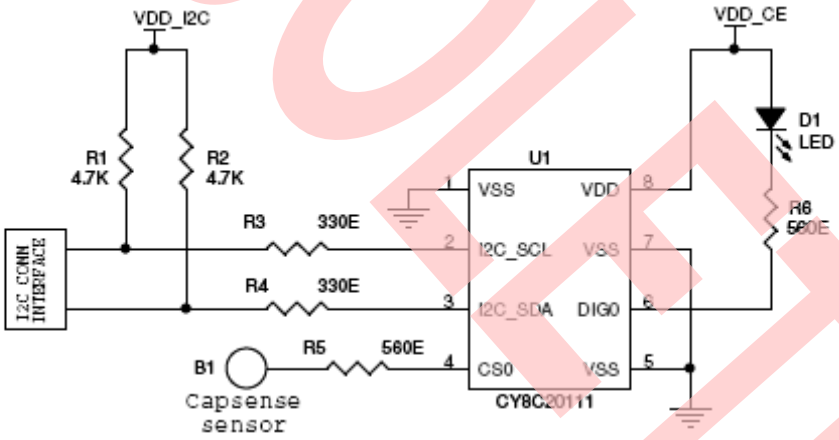


Figure 6. Circuit-4: Compatibility with 1.8 V I²C Signaling [2, 3]



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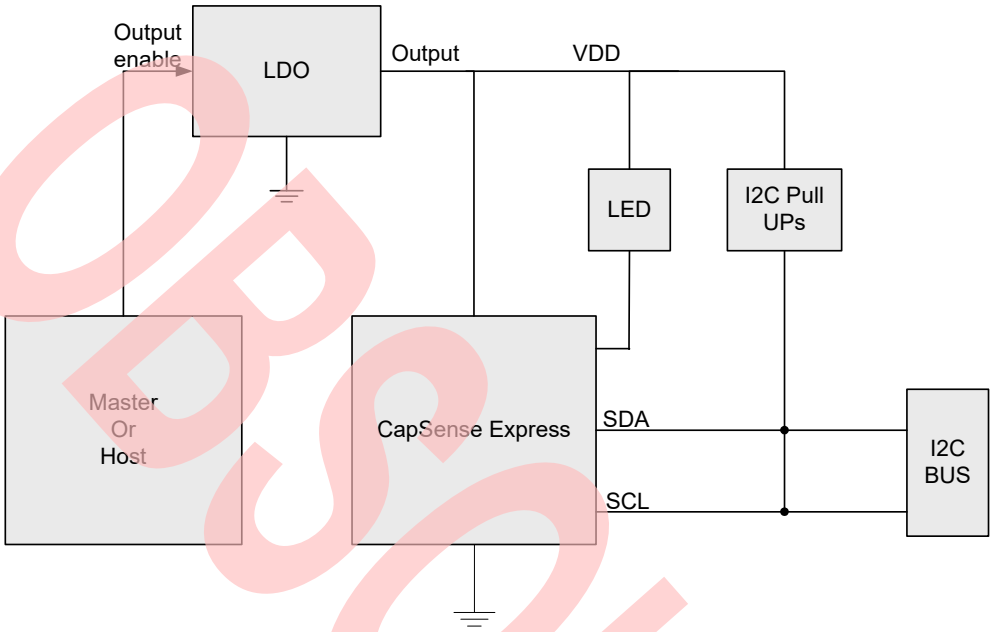
Note
2. 1.8 V ≤ V_{DD}_I2C ≤ V_{DD}_CE and 2.4 V ≤ V_{DD}_CE ≤ 5.25 V.
3. The I2C drive mode of the CapSense device should be configured properly before using in an I2C environment with external pull-ups. Please refer to I2C_ADDR_DM register and its factory setting.

Typical Circuits *(continued)*

Figure 7. Circuit-5: Powering Down CapSense Express Device for Low Power Requirements [4]



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Note

4. For low power requirements, if VDD is to be turned off, the above concept can be used. The VDDs of CapSense Express, I2C pull-ups, and LEDs must be from the same source. Turning off the VDD ensures that no signal is applied to the device while it is unpowered. The I2C signals should not be driven high by the master in this situation. If a port pin or group of port pins can cater to the power supply requirement of the circuit, the LDO can be avoided.

Operating Modes

Normal Mode

In normal mode of operation, the acknowledgment time is optimized. The timings remain approximately the same for different configurations of the slave. To reduce the acknowledgment times in normal mode, the registers 0x07, 0x08, 0x11, 0x50, 0x51, 0x5C, 0x5D are given only read access. Writing to these registers can be done only in setup mode.

Setup Mode

All registers have read and write access (except those which are read only) in this mode. The acknowledgment times are longer compared to normal mode. When CapSense scanning is disabled (command code 0x0A in command register 0xA0), the acknowledgment times can be improved to values similar to the normal mode of operation.

I²C Interface

The CapSense Express devices support the industry standard I²C protocol, which can be used to:

- Configure the device
- Read the status and data registers of the device
- Control device operation
- Execute commands

The I²C address can be modified during configuration.

I²C Device Addressing

The device uses a seven bit addressing protocol. The I²C data transfer is always initiated by the master sending one byte address; first 7-bit contains address and LSb indicates the data transfer direction. Zero in the LSb indicates the write transaction form master and one indicates read transfer by the master. Table 1 shows example for different I²C addresses.

Table 1. I²C Addresses

7-bit Slave Address (in Dec)	D7	D6	D5	D4	D3	D2	D1	D0	8-bit Slave Address (in Hex)
1	0	0	0	0	0	0	1	0(W)	02
1	0	0	0	0	0	0	1	1(R)	03
75	1	0	0	1	0	1	1	0(W)	96
75	1	0	0	1	0	1	1	1(W)	97

I²C Clock Stretching

"Clock stretching" or "bus stalling" in I²C communication protocol is a state in which the slave holds the SCL line low to indicate that it is busy. In this condition, the master is expected to wait until the SCL is released by the slave.

When an I²C master communicates with the CapSense Express device, the CapSense Express stalls the I²C bus after the reception of each byte (that is, just before the ACK/NAK bit) until processing of the byte is complete and critical internal functions are executed. Use a fully I²C compliant master to communicate with the CapSense Express device.

An I²C master which does not support clock stretching (a bit banged software I²C Master) must wait for a specific amount of time specified (as shown in the section Format for Register Write and Read) for each register write and read operation before the next bit is transmitted. It is mandatory to check the SCL status (it should be high) before I²C master initiates any data transfer with CapSense Express. If the master fails to do so and continues to communicate, the communication is erroneous.

The following diagrams represent the ACK time delays shown in the Register Map on page 7.

Also note that, while using CapSense Express Devices on an I2C bus, I2C master should not generate a start or stop condition in the I2C bus before CapSense Express device generating acknowledgement (ACK/NCK) for the previous transaction. An acknowledgement state produced by the CapSense Express Device for the previous data transfer after start condition for new data transfer by the master may produce unexpected behavior from CapSense Express I2C slave interface.

Figure 8. Write ACK Time Representation

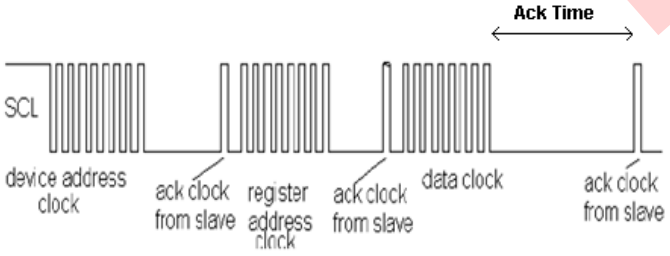

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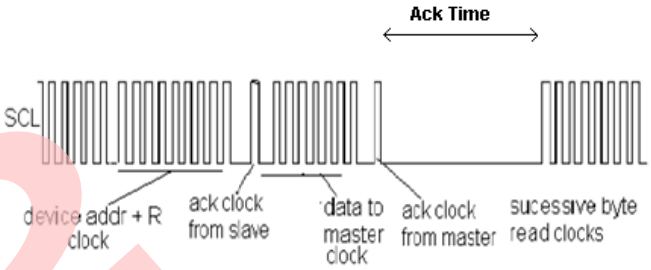
Figure 9. Read ACK Time Representation



Format for Register Write and Read

Register write format

Start	Slave Addr + W	A	Reg Addr	A	Data	A	Data	A	. . . . .	Data	A	Stop		

Register read format

Start	Slave Addr + W	A	Reg Addr	A	Stop							
Start	Slave Addr + R	A	Data	A	Data	A	. . . . .	Data	N	Stop		

Legends

Master	A – ACK
Slave	N – NAK

Registers

Register Conventions

Convention	Description
RW	Register have both read and write access
R	Register have only read access
WPR	Write register with pass code
FD	Factory defaults

OBSOLETE

Register Map

Name	Register Address (in Hex)	Access	Writable Only in Setup Mode [5]	Factory Default Values of Registers (in Hex)		I²C Max ACK Time in Normal Mode (ms) [6]	I²C Max ACK Time in Setup Mode (ms) [6]	Page No.
				1 Button	2 Button			
OUTPUT_PORT	04	W	–	01	03	0.10	–	13
CS_ENABLE	07	RW	Yes	01	03	–	11	13
DIG_ENABLE	08	RW	Yes	01	03	–	11	14
SET_STRONG_DM	11	RW	Yes	01	03	–	11	14
OP_SEL_0	1C	RW	–	82	82	0.12	11	15
LOGICAL_OPR_INPUT0	1E	RW	–	01	01	0.12	11	15
OP_SEL_1 [7]	21	RW	–		82	0.12	11	15
LOGICAL_OPR_INPUT1 [7]	23	RW	–		02	0.12	11	15
CS_NOISE_TH	4E	RW	–	28	28	0.11	11	16
CS_BL_UPD_TH	4F	RW	–	64	64	0.11	11	16
CS_SETL_TIME	50	RW	Yes	A0	A0	–	35	16
CS_OTH_SET	51	RW	Yes	00	00	–	35	17
CS_HYSTERISIS	52	RW	–	0A	0A	0.11	11	17
CS_DEBOUNCE	53	RW	–	03	03	0.11	11	18
CS_NEG_NOISE_TH	54	RW	–	14	14	0.11	11	18
CS_LOW_BL_RST	55	RW	–	14	14	0.11	11	18
CS_FILTERING	56	RW	–	20	20	0.11	11	19
CS_SCAN_POS_0	5C	RW	Yes	00	00	–	11	19
CS_SCAN_POS_1 [7]	5D	RW	Yes		01	–	11	19
CS_FINGER_TH_0	66	RW	–	64	64	0.14	11	20
CS_FINGER_TH_1 [7]	67	RW	–		64	0.14	11	20
CS_IDAC_0	70	RW	–	0A	0A	0.14	11	20
CS_IDAC_1 [7]	71	RW	–		0A	0.14	11	20
I2C_ADDR_LOCK	79	RW	–	01	01	0.11	11	20
DEVICE_ID	7A	R	–	11	21	0.11	11	21
DEVICE_STATUS	7B	R	–	03	03	0.11	11	21
I2C_ADDR_DM	7C	RW	–	80	80	0.11	11	22
CS_READ_BUTTON	81	RW	–	81	81	0.12	11	22
CS_READ_BLM	82	R	–	NA	NA	0.12	11	23
CS_READ_BLL	83	R	–	NA	NA	0.12	11	23
CS_READ_DIFFM	84	R	–	NA	NA	0.12	11	23
CS_READ_DIFFL	85	R	–	NA	NA	0.12	11	23
CS_READ_RAWM	86	R	–	NA	NA	0.12	11	23
CS_READ_RAWL	87	R	–	NA	NA	0.12	11	23

Notes
5. These registers are writable only after entering into setup mode. All other registers are available for read and write in normal and setup mode.
6. The Ack times specified are 1x I2C Ack times.
7. These registers are available only in CY8C20121 device.

OBSOLETE

Register Map *(continued)*

Name	Register Address (in Hex)	Access	Writable Only in Setup Mode [5]	Factory Default Values of Registers (in Hex)		I²C Max ACK Time in Normal Mode (ms) [6]	I²C Max ACK Time in Setup Mode (ms) [6]	Page No.
				1 Button	2 Button			
CS_READ_STATUS	88	R	–	NA	NA	0.12	11	24
COMMAND_REG	A0	W	–	00	00	0.10	11	24

CapSense Express Commands

Command [8]	Description	Executable Mode	Duration the Device is NOT Accessible after ACK (in ms) [9]
W 00 A0 00	Get firmware revision	Setup/Normal	0
W 00 A0 01	Store current configuration to NVM	Setup/Normal	120
W 00 A0 02	Restore factory configuration	Setup/Normal	120
W 00 A0 03	Write NVM POR defaults	Setup/Normal	120
W 00 A0 04	Read NVM POR defaults	Setup/Normal	5
W 00 A0 05	Read current configurations (RAM)	Setup/Normal	5
W 00 A0 06	Reconfigure device (POR)	Setup	5
W 00 A0 07	Set Normal mode of operation	Setup/Normal	0
W 00 A0 08	Set Setup mode of operation	Setup/Normal	0
W 00 A0 09	Start scan	Setup/Normal	10
W 00 A0 0A	Stop scan	Setup/Normal	5
W 00 A0 0B	Get CapSense scan status	Setup/Normal	0

OBSOLETE

Notes
8. 'W' indicates the write transfer. The next byte of data represents the 7-bit I²C address.
9. The Ack times specified are 1x I2C Ack times.

OUTPUT_STATUS

Output Status Register

OUTPUT_STATUS: 00h

1 Button	7	6	5	4	3	2	1	0
Access: FD								R:01
Bit Name								STS[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							R:03	
Bit Name							STS[1:0]	

The Output Status register represents the actual logical levels on the output pins.

Bit	Name	Description
1:0	STS [1:0]	Used to represent the output status 0 Output low 1 Output high

OUTPUT_PORT

Output Port Register

OUTPUT_PORT: 04h

1 Button	7	6	5	4	3	2	1	0
Access: FD								W:01
Bit Name								DIG[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							W:03	
Bit Name							DIG[1:0]	

This register is used to write data to DIG output port. Pins defined as output of combinational logic (in OP_SEL_x register) cannot be changed using this register.

Bit	Name	Description
1:0	DIG [1:0]	A bit set in this register sets the logic level of the output. 0 Logic ‘0’ 1 Logic ‘1’

CS_ENABLE

Select CapSense Input Register

CS_ENABLE: 07h

(Writable only in Setup mode)

1 Button	7	6	5	4	3	2	1	0
Access: FD								RW:01
Bit Name								CS[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:03	
Bit Name							CS[1:0]	

OBSOLETE

This register is used to enable CapSense inputs. **This register should be set before setting finger threshold (0x66, 0x67) and IDAC setting (0x70, 0x71) registers.**

Bit	Name	Description
1:0	CS [1:0]	These bits are used to enable CapSense inputs. 0 Disable CapSense input 1 Enable CapSense input

DIG_ENABLE

Select DIG Output Register

GPO_ENABLE: 08h

(Writable only in Setup mode)

1 Button	7	6	5	4	3	2	1	0
Access: FD								RW:01
Bit Name								DIG[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:03	
Bit Name							DIG [1:0]	

This register is used to enable DIG (Digital) outputs. If DIG output is enabled, the strong drive mode register (11h) should also be set. If DIG output is disabled the drive mode of these pins is High Z.

Bit	Name	Description
1:0	DIG [1:0]	These bits are used to enable DIG outputs. 0 Disable DIG output 1 Enable DIG output

SET_STRONG_DM

Sets Strong Drive Mode for DIG Outputs.

SET_STRONG_DM: 11h

(Writable only in Setup mode)

1 Button	7	6	5	4	3	2	1	0
Access: FD								RW:01
Bit Name								DM [0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:03	
Bit Name							DM [1:0]	

This register sets strong drive mode for DIG (Digital) outputs. To set strong drive mode the pin should be enabled as GP output.

Bit	Name	Description
1:0	DM [1:0]	These bits are used to set the strong drive mode to DIG outputs. 0 Strong drive mode not set 1 Strong drive mode set

OBSOLETE

OP_SEL_x

Logic Operation Selection Registers

OP_SEL_0: 1Ch OP_SEL_1: 21h (Not available for 1 Button)

1/2Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0						RW: 0	RW: 0
Bit Name	Op_En						InvOp	Operator

This register is used to enable logic operation on GP outputs. OP_SEL_0 should be configured to get the logic operation output on DIG0 output and OP_SEL_1 for DIG1 output. Write to these registers during the disable state of respective DIG output pins does not have any effect.

The input to the logic operation can be selected in LOGIC_OPRX registers. The selected inputs can be ORed or ANDed. The output of logic operation can also be inverted.

Bit	Name	Description
7	Op_En	This bit enables or disables logic operation. 0 Disable logic operation 1 Enable logic operation
1	InvOp	This bit enables or disables logic operation output inversion. 0 Logic operation output not inverted 1 Logic operation output inverted
0	Operator	This bit selects which operator should be used to compute logic operation. 0 Logic operator OR is used on inputs 1 Logic operator AND is used on inputs

LOGICAL_OPR_INPUTx

Selects Input for Logic Operation

LOGICAL_OPR_INPUT0: 1Eh LOGICAL_OPR_INPUT1: 23h (Not available for 1 button)

LOGICAL_OPR_INPUT0

1 Button	7	6	5	4	3	2	1	0
Access: FD								RW:01
Bit Name								CSL[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:01	
Bit Name							CSL [1:0]	

LOGICAL_OPR_INPUT1

2 Button	7	6	5	4	3	2	1	0
Access: FD							RW:02	
Bit Name							CSL [1:0]	

These registers are used to give the input to logic operation block. The inputs can be only CapSense input status.

Bit	Name	Description
1:0	CSL [1:0]	These bits selects the input for logic operation block.

OBSOLETE

CS_NOISE_TH

Noise Threshold Register

CS_NOISE_TH: 4Eh

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:28							
Bit Name	NT[7:0]							

This register sets the noise threshold value. For individual sensors, count values above this threshold do not update the baseline. This count is relative to baseline. This parameter is common for all sensors.

The range is 3 to 255 and it should satisfy the equation NT < Min (Finger Threshold – Hysteresis – 5). Recommended value is 40% of finger threshold.

Bit	Name	Description
7:0	NT [7:0]	These bits are used to set the noise threshold value.

CS_BL_UPD_TH

Baseline Update Threshold Register

CS_BL_UPD_TH: 4Fh

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:64							
Bit Name	BLUT[7:0]							

When the new raw count value is above the current baseline and the difference is below the noise threshold, the difference between the current baseline and the raw count is accumulated into a “bucket.” When the bucket fills, the baseline increments and the bucket is emptied. This parameter sets the threshold that the bucket must reach for the baseline to increment. In other words, lower value provides faster baseline update rate and vice versa. This parameter is common for all sensors.

The range is 0 to 255.

Bit	Name	Description
7:0	BLUT [7:0]	These bits set the threshold that the bucket must reach for baseline to increment.

CS_SETL_TIME

Settling Time Register

CS_SETL_TIME: 50h

(Writable only in Setup mode)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:A0							
Bit Name	STLNG_TM[7:0]							

The settling time parameter controls the duration of the capacitance-to-voltage conversion phase. The parameter setting controls a software delay that allows the voltage on the integrating capacitor to stabilize. This parameter is common for all sensors.

This register should be set before setting finger threshold (0x66, 0x67) and IDAC setting (0x70, 0x71) registers.

The range is 2 to 255.

Bit	Name	Description
7:0	STLNG_TM [7:0]	These bits are used to set the settling time value.

OBSOLETE

CS_OTH_SET

CapSense Clock Select, Sensor Auto Reset Register

CS_OTH_SET: 51h

(Writable only in Setup mode)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD		RW: 00			RW: 0			
Bit Name		CS_CLK[1:0]			Sns_Ar			

The registers set the CapSense module frequency of operation and enables or disables the sensor auto reset.

CS_CLK bits provides option to select variable clock input for the CapSense block. A sensor design having higher paratactic requires lower clock for better performance and vice versa.

Sensor Auto Reset determines whether the baseline is updated at all times or only when the signal difference is below the noise threshold. When set to '1' (enabled), the baseline is updated constantly. This setting limits the maximum time duration of the sensor, but it prevents the sensors from permanently turning on when the raw count suddenly rises without anything touching the sensor. This sudden rise can be caused by a large power supply voltage fluctuation, a high energy RF noise source, or a very quick temperature change. When the parameter is set to '0' (disabled), the baseline is updated only when raw count and baseline difference is below the noise threshold parameter. This parameter may be enabled unless there is a demand to keep the sensors in the on state for a long time. This parameter is common for all sensors.

Bit	Name	Description
6:5	CS_CLK[1:0]	These bits selects the CapSense clock. 00 IMO 01 IMO/2 10 IMO/4 11 IMO/8
3	Sns_Ar	This bit is used to enable or disable sensor auto reset. 0 Disable Sensor auto reset 1 Enable Sensor auto reset

CS_HYSTERISIS

Hysteresis Register

CS_HYSTERISIS: 52h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:0A							
Bit Name	HYS[7:0]							

The Hysteresis parameter adds to or subtracts from the finger threshold depending on whether the sensor is currently active or inactive. If the sensor is off, the difference count must overcome the 'finger threshold + hysteresis'. If the sensor is on, the difference count must go below the 'finger threshold – hysteresis'. It is used to add debouncing and "stickiness" to the finger detection algorithm. This parameter is common for all sensors.

Possible values are 0 to 255. However, the setting must be lower than the finger threshold parameter setting. Recommended value for hysteresis is 15 percent of finger threshold.

Bit	Name	Description
7:0	HYS [7:0]	These bits are used to set the hysteresis value.

OBSOLETE

CS_DEBOUNCE

Debounce Register.

CS_DEBOUNCE: 53h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:0A							
Bit Name	DB[7:0]							

The Debounce parameter adds a debounce counter to the 'sensor active transition'. For the sensor to transition from inactive to active, the consecutive samples of difference count value must stay above the 'finger threshold + hysteresis' for the number specified. This parameter is common for all sensors.

Possible values are 1 to 255. A setting of '1' provides no debouncing.

Bit	Name	Description
7:0	DB [7:0]	These bits are used to set the debounce value.

CS_NEG_NOISE_TH

Negative Noise Threshold Register

CS_NEG_NOISE_TH: 54h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:0A							
Bit Name	NNT[7:0]							

This parameter adds a negative difference count threshold. If the current raw count is below the baseline and the difference between them is greater than this threshold, the baseline is not updated. However, if the current raw count stays in the low state (difference greater than the threshold) for the number of samples specified by the Low Baseline Reset parameter, the baseline is reset. This parameter is common for all sensors.

Bit	Name	Description
7:0	NNT [7:0]	These bits are used to set the negative noise value.

CS_LOW_BL_RST

Low Baseline Reset Register

CS_LOW_BL_RST: 55h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW:0A							
Bit Name	LBR[7:0]							

This parameter works together with the Negative Noise Threshold parameter. If the sample count values are below the baseline minus the negative noise threshold for the specified number of samples, the baseline is set to the new raw count value. It essentially counts the number of abnormally low samples required to reset the baseline. It is generally used to correct the finger-on-at-startup condition. This parameter is common for all sensors.

Bit	Name	Description
7:0	LBR [7:0]	These bits are used to set the Low Baseline Reset value.

OBSOLETE

CS_FILTERING

CapSense Filtering Register

CS_FILTERING: 56h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0		RW: 1	RW: 0			RW: 00	
Bit Name	RstBl		I2C_DS	Avg_En			Avg_Order[1:0]	

This register provides an option for forced baseline reset and to enable and configure two different types of software filters.

Bit	Name	Description
7	RstBl	This bit resets all the baselines and it is auto cleared to '0'. 0 All Baselines are not reset 1 All baselines are reset
5	I2C_DS	When this bit is set to '1' the CapSense scan sample is dropped if I^2C communication was active during scanning. 0 Disable the I^2C drop sample filer 1 Enable the I^2C drop sample filter
4	Avg_En	This bit enables average filter on raw counts. 0 Disable the average filter 1 Enable the average filter
[1:0]	Avg_Order[1:0]	These bits are used to select the number of CapSense samples to average: Avg_Order[1:0] in Hex / Samples to Average 00 / 2 01 / 4 10 / 8 11 / 16

CS_SCAN_POS_x

Scan Position Registers

CS_SCAN_POS_0: 5Ch

(Writable only in Setup mode)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD								RW: 0
Bit Name								Scan_Pstn

CS_SCAN_POS_1: 5Dh (Not available for 1 Button)

(Writable only in Setup mode)

2 Button	7	6	5	4	3	2	1	0
Access: FD								RW: 1
Bit Name								Scan_Pstn

This register is used to set the position of the sensors in the switch table for proper scanning sequence because the CapSense sensors are scanned in sequence.

This register should be set after setting 0x07, 0x50, and 0x51 registers.

Bit	Name	Description
0	Scan_Pstn	This bit sets the scan position.

OBSOLETE

CS_FINGER_TH_x

Finger Threshold Registers

CS_FINGER_TH_0: 66h CS_FINGER_TH_1: 67h (Not available in 1 Button)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 64							
Bit Name	FT[7:0]							

This register sets the finger threshold value for CapSense inputs. Possible values are 3 to 255. This parameter should be configured individually for each CapSense inputs.

This register should be set after setting 0x07, 0x50, and 0x51 registers.

Bit	Name	Description
[7:0]	FT [7:0]	These bit set the finger threshold for CapSense inputs.

CS_IDAC_x

IDAC Setting Registers

CS_IDAC_0: 70h CS_IDAC_1: 71h (Not available in 1 Button)

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0A							
Bit Name	IDAC[7:0]							

The IDAC register controls the sensitivity of the CapSense algorithm. This register is used to tune the CapSense input for specific design or overlays. Decreasing the value of this register increases the sensitivity of the CapSense buttons and vice versa. Decreasing the value of IDAC increases noise and vice versa.

Possible values are 1 to 255. If the value is set to 0 then the value is reset to default value 10.

The recommended value is greater than 4. Setting value ≤ 4 creates excessive amount of noise.

This register should be set after setting 0x07, 0x50, and 0x51 registers.

Bit	Name	Description
[7:0]	IDAC [7:0]	These bit set the IDAC values.

I2C_ADDR_LOCK

I2C Address Lock Registers

I2C_ADDR_LOCK: 79h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD								WPR: 0
Bit Name								I2CAL

This register is used to unlock and lock the I^2C address register (7Ch) access. The device I^2C address should be modified by writing new address to register 7Ch after unlocking the access using this register. Write to the 7C register during the locked state does not have any effect and the new address take effect only after the access is locked.

To lock or unlock the I^2C AL bit, the following three bytes must be written to register 79h:

- unlock I2CAL: 3Ch A5h 69h
- lock I2CAL: 96h 5Ah C3h

Reading the I2CAL bit from register 79h indicates the current access state.

Bit	Name	Description
0	I2CAL	This bit gives the lock/unlock status of I^2C address. 0 Unlocked 1 Locked

OBSOLETE

DEVICE_ID

Device ID Register

DEVICE_ID: 7Ah

1 Button	7	6	5	4	3	2	1	0
Access: FD	R: 11							
Bit Name	DEV_ID[7:0]							

2 Button	7	6	5	4	3	2	1	0
Access: FD	R: 21							
Bit Name	DEV_ID[7:0]							

This register contains the device and product ID. The device and product ID corresponds to “xx” in CY8C201xx.

Bit	Name	Description
7:0	DEV_ID [7:0]	These bits contain the device and product ID.

Part No	Device/Product ID
CY8C20111	11
CY8C20121	21

DEVICE_STATUS

Device Status Register

DEVICE_STATUS: 7Bh

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	R : 00		R: 0	R : 0	R: 0		R: 0	R: 0
Bit Name	Ip_Volt[1:0]		IRES	Load_FD	No_NVM_Wr		CSE	DIGE

This register contains the device status.

Bit	Name	Description
7:6	Ip_Volt [1:0]	Supply voltage is automatically detected and these bits are set accordingly.

Ip_Volt[1:0]	Supply Voltage
00	5
01	3.3
10	2.7
11	Reserved

5	IRES	When set to ‘1’, this bit indicates that an internal reset occurred. 0 indicates the last system reset was not internal reset 1 indicates the last system reset was internal reset
4	Load_FD	This bit indicates whether factory defaults are loaded during power-up. 0 User default configuration is loaded during power-up 1 Factory default configuration is loaded during power-up
3	No_NVM_Wr	When set to ‘1’, this bit indicates that the supply voltage applied to the device Is too low for a write to nonvolatile memory operation, and no write is performed. This bit must be checked before any Store or Write POR command.
1	CSE	This bit indicates whether CapSense function is enabled or disabled. 0 Functionality of CapSense block is disabled 1 Functionality of CapSense block is enabled
0	DIGE	This bit indicates whether GP Output function is enabled or disabled. 0 Functionality of Digital output block is disabled 1 Functionality of Digital output block is enabled

OBSOLETE

I2C_ADDR_DM

Device I²C Address and I²C Pin Drive Mode Register

I2C_ADDR_DM: 7Ch

1 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0	RW: 00						
Bit Name	I2CIP_EN	I2C_ADDR[6:0]						

This register sets the drive mode of I²C pins and I²C slave address. To write to this register, register 79h must first be unlocked. The value written to register 7Ch is applied only after locking register 79h again.

Bit	Name	Description
7	I2CIP_EN	This bit is used to set the I²C pins drive mode. 0 Internal pull-up enabled 1 Internal pull-up disabled
6:0	I2C_ADDR [6:0]	Used to set the device I²C address.

CS_READ_BUTTON

Button Select Register

CS_READ_BUTTON: 81h

1 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0							RW: 0
Bit Name	RD_EN							CSBN[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD	RW: 0						RW: 00	
Bit Name	RD_EN						CSBN[1:0]	

The scan result of a CapSense input (raw count, difference count, and baseline) can be read only for one input at a time using 82h–87h registers. This register is used to select a CapSense input to read the raw count, difference count, and baseline. Only the pins defined as CapSense inputs in register 07h can be used with this register. Trying to select other pins not defined as CapSense does not have any change.

Bit	Name	Description
7	RD_EN	This bit enables the CapSense raw data reading. 0 Disable CapSense scan result reading 1 Enable CapSense scan result reading
1:0	CSBN [1:0]	These bits decide which CapSense button scan result are read. When writing to this register, the bitmask must contain only one bit set to '1', otherwise the data is discarded.

CSBN [1:0]	CapSense Button No
01	1
10	2

OBSOLETE

CS_READ_BLx

Baseline Value MSB/LSB Registers

CS_READ_BLM: 82h CS_READ_BLL: 83h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	R: 00							
Bit Name	BL [7:0]							

Reading from this register returns the 2-byte current baseline value for the selected CapSense input.

Bit	Name	Description
7:0	BL [7:0]	These bits represent the baseline value.

CS_READ_DIFFx

Difference Count Value MSB/LSB Registers

CS_READ_DIFFM: 84h CS_READ_DIFFL: 85h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	R: 00							
Bit Name	DIF [7:0]							

Reading from this register returns the 2-byte current difference count for the selected CapSense input.

Bit	Name	Description
7:0	DIF [7:0]	These bits represent the sensor difference count.

CS_READ_RAWx

Difference Count Value MSB/LSB Registers

CS_READ_RAWM: 86h CS_READ_RAWL: 87h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	R: 00							
Bit Name	RC [7:0]							

Reading from this register returns the 2-byte current raw count value for the selected CapSense input.

Bit	Name	Description
7:0	RC [7:0]	These bits represent the raw count value.

OBSOLETE

CS_READ_STATUS

Sensor On Status Register

CS_READ_STATUS: 88h

1 Button	7	6	5	4	3	2	1	0
Access: FD								R: 0
Bit Name								BT_ST[0]

2 Button	7	6	5	4	3	2	1	0
Access: FD							R: 00	
Bit Name							BT_ST[1:0]	

This register gives the sensor ON/OFF status. A bit '1' indicates sensor is ON and '0' indicates sensor is OFF.

Bit	Name	Description
1:0	BT_ST [1:0]	These bits used to represent sensor status. 0 Sensor OFF 1 Sensor ON

COMMAND_REG

Command Register

COMMAND_REG: A0h

1/2 Button	7	6	5	4	3	2	1	0
Access: FD	W: 00							
Bit Name	Cmnd [7:0]							

Commands are executed by writing the command code to the command register.

Bit	Name	Description
7:0	Cmnd [7:0]	Refer to the following table for command register opcodes.

Table 2. Command Register Opcodes

Command Code	Name	Description
00h	Get Firmware Revision	The I^2C buffer is loaded with the one byte firmware revision value. Reading one byte after writing this command returns the firmware revision. The upper nibble of the firmware revision byte is the major revision number and the lower nibble is the minor revision number.
01h	Store Current Configuration to NVM	The current register settings are saved in nonvolatile memory (flash). This setting is automatically loaded after the next device reset/power-up or if the Reconfigure Device (06h) command is issued.
02h	Restore Factory Configuration	Replaces the saved user configuration with the factory default configuration. Current settings are unaffected by this command. New settings are loaded after the next device reset/power-up or if the 06h command is issued.

OBSOLETE

Table 2. Command Register Opcodes *(continued)*

Command Code	Name	Description
03h	Write POR Defaults	Sends new power-up defaults to the CapSense controller without changing current settings unless the 06h command is issued afterwards. This command is followed by 123 data bytes according to the POR Default Data Structure table. The CRC is calculated as the XOR of the 122 data bytes (00h-79h). If the CRC check fails or an incomplete block is sent, the slave responds with an ACK and the data is NOT saved to flash. To define new POR defaults: ■ Write command 03h ■ Write 122 data bytes with new values of registers (use the _flash.iic file generated from s/w tool) ■ Write one CRC byte calculated as XOR of previous 122 data bytes
04h	Read POR Defaults	Reads the POR settings stored in the nonvolatile memory. To read POR defaults: ■ Write command 04h ■ Read 122 data bytes ■ Read one CRC byte
05h	Read Device Configuration (RAM)	Reads the current device configuration. Gives the user “flat-address-space” access to all device settings. To read device configuration: ■ Write command 05h ■ Read 122 data bytes ■ Read one CRC byte
06h	Reconfigure Device (POR)	Immediately reconfigures the device with actual POR defaults from flash. Has the same effect on the registers as a POR. This command can only be executed in setup operation mode (command code 08).
07h	Set Normal Operation Mode	Sets the device in normal operation mode. In this mode, CapSense pin assignments cannot be modified; settling time, IDAC setting, external capacitor, and sensor auto-reset also cannot be modified.
08h	Set Setup Operation Mode	Sets the device in setup operation mode. In this mode, CapSense pin assignments can be changed along with other parameters.
09h	Start CapSense Scanning	Allows the user to start CSA scanning after it has been stopped using command 0x0A. Note that at POR, scanning is enabled and started by default if one or more sensors are enabled.
0Ah	Stop CapSense Scanning	Allows the user to stop CSA scanning. A system host controller might initiate this command before powering down the device to make sure that during power-down no CapSense touches are detected. When CSA scanning is stopped by the user and the device is still in the valid V_{CC} operating range, the following behavior is supported: ■ Any change to configuration can still be done (as long as V_{CC} is in operating range). ■ Command code 0x06 overrides the status of stop/scan by enabling and starting CSA scanning if one or more sensors are enabled. ■ CapSense read-back values return 0x00.
0Bh	Returns CapSense Scanning Status	The I^2C buffer is loaded with the one-byte CSA scanning status value. After writing the value 0Bh to the A0h register, reading one byte returns the CSA scanning status. It returns the LVD_STOP_SCAN and STOP_SCAN bits. LVD_STOP_SCAN is bit 3 - Set when CSA is stopped because V_{CC} is outside the valid operating range. STOP_SCAN is bit 2 - Set when CSA is stopped by the user by writing command 0x0A.

OBSOLETE

Layout Guidelines and Best Practices

Table 3 provides a set of high level rules for board design. Cypress also provides an extensive set of design guidelines for CapSense board designs. Refer to the Getting Started with CapSense Design Guide for complete system guidelines.

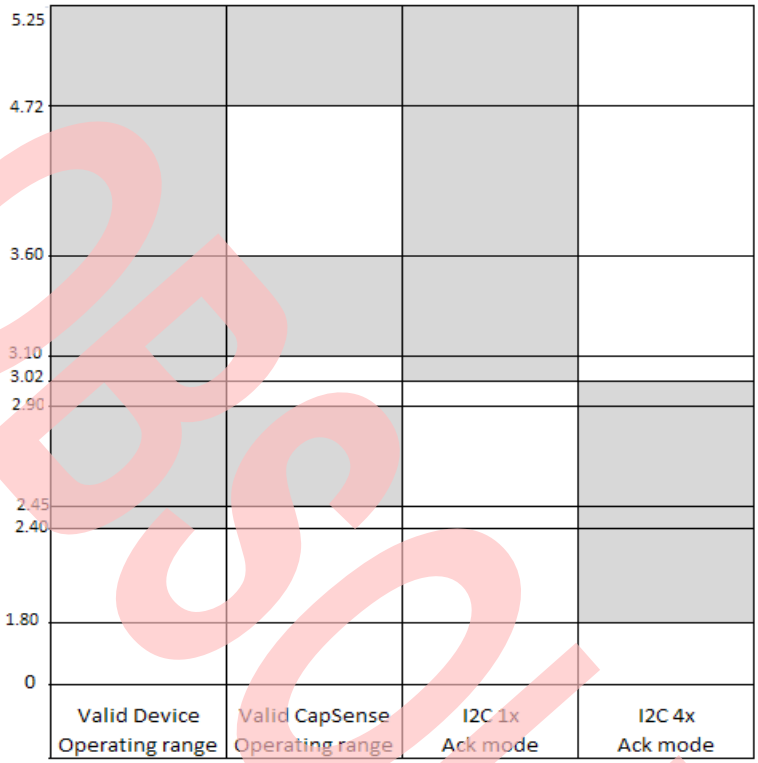
Table 3. Layout Guidelines and Best Practices

Sl. No.	Category	Min	Max	Recommendations/Remarks
1	Button Shape	–	–	Solid round pattern, round with LED hole, rectangle with round corners
2	Button Size	5 mm	15 mm	10 mm
3	Button Button Spacing	= Button Ground Clearance	–	8 mm
4	Button Ground Clearance	0.5 mm	2 mm	Button ground clearance = Overlay Thickness
5	Ground Flood – Top Layer	–	–	Hatched ground 7 mil trace and 45 mil grid (15% filling)
6	Ground Flood – Bottom Layer	–	–	Hatched ground 7 mil trace and 70 mil grid (10% filling)
7	Trace Length from Sensor to PSoC - Buttons	–	200 mm	< 100 mm.
8	Trace Width	0.17 mm	0.20 mm	0.17 mm (7 mil)
9	Trace Routing	–	–	Traces should be routed on the non sensor side. If any non CapSense trace crosses CapSense trace, ensure that intersection is orthogonal.
10	Via Position for the Sensors	–	–	Via should be placed near the edge of the button/slider to reduce trace length thereby increasing sensitivity.
11	Via Hole Size for Sensor Traces	–	–	10 mil
12	No. of Via on Sensor Trace	1	2	1
13	CapSense Series Resistor Placement	–	10mm	Place CapSense series resistors close to PSoC for noise suppression.CapSense resistors have highest priority place them first.
14	Distance between any CapSense Trace to Ground Flood	10 mil	20 mil	20 mil
15	Device Placement	–	–	Mount the device on the layer opposite to sensor. The CapSense trace length between the device and sensors should be minimum
16	Placement of Components in 2 Layer PCB	–	–	Top layer-sensor pads and bottom layer-PSoC, other components and traces.
17	Placement of Components in 4 Layer PCB	–	–	Top layer-sensor pads, second layer – CapSense traces, third layer-hatched ground, bottom layer- PSoC, other components and non CapSense traces
18	Overlay Material	–	–	Should to be non conductive material. Glass, ABS Plastic, Formica
19	Overlay Adhesives	–	–	Adhesive should be non conductive and dielectrically homogenous. 467MP and 468MP adhesives made by 3M are recommended.
20	LED Back Lighting	–	–	Cut a hole in the sensor pad and use rear mountable LEDs. Refer Operating Voltages on page 27.
21	Board Thickness	–	–	Standard board thickness for CapSense FR4 based designs is 1.6 mm.

The Recommended maximum overlay thickness is 2 mm. For more details refer to the section “The Integrating Capacitor (Cint)” in AN53490.

OBSOLETE

Operating Voltages



For details on I2C 1x Ack time, refer Table on page 11 and Table on page 12. I2C 4x Ack time is approximately four times the values mentioned in these tables.

CapSense Constraints

Parameter	Min	Typ	Max	Units	Notes
Parasitic Capacitance (C_P) of the CapSense Sensor	–	–	30	pF	–
Supply Voltage Variation (V_{DD})	–	–	± 5%		–

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Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C (0 °C to 50 °C). Extended duration storage temperatures above 65 °C degrade reliability
$T_{BAKETEMP}$	Bake Temperature	–	125	See Package label	°C	–
$t_{BAKETIME}$	Bake Time	See package label	–	72	Hours	–
T_A	Ambient temperature with power applied	–40	–	+85	°C	–
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	–
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	–
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	–
I_{MIO}	Maximum current into any GPIO pin	–25	–	+50	mA	–
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch up current	–	–	200	mA	–

Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_A	Ambient temperature	–40	–	+85	°C	–
T_J	Junction temperature	–40	–	+100	°C	–

OBSOLETE

Electrical Specifications

DC Electrical Specifications

DC Chip Level Specifications

Table 4. DC Chip Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	–
I_{DD}	Supply current	–	1.5	2.5	mA	Conditions are V_{DD} = 3.10 V, T_A = 25 °C

DC GPIO Specifications

Table 5 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.10 V to 3.6 V –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 5. 5-V and 3.3-V DC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage	V_{DD} – 0.2	–	–	V	I_{OH} ≤ 10 µA/pin, V_{DD} ≥ 3.10 V
V_{OH2}	High output voltage	V_{DD} – 0.9	–	–	V	I_{OH} = 1 mA/pin, V_{DD} ≥ 3.10 V
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 20 mA/pin, V_{DD} > 3.10 V, maximum of 40 mA sink current
I_{OH}	High output current	0.01	–	1	mA	V_{DD} ≥ 3.1 V
I_{OL1}	Low output current on Port 0 pins	–	–	10	mA	V_{DD} ≥ 3.1 V, maximum of 40 mA sink current
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25 °C.

Table 6 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4 V to 2.90 V and –40 °C < T_A < 85 °C, respectively. Typical parameters apply to 2.7 V at 25 °C and are for design guidance only.

Table 6. 2.7-V DC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage	V_{DD} – 0.2	–	–	V	I_{OH} ≤ 10 µA/pin
V_{OH2}	High output voltage	V_{DD} – 0.5	–	–	V	I_{OH} = 0.2 mA/pin
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 10 mA/pin, maximum of 20 mA sink current
I_{OH}	High output current	0.01	–	0.2	mA	V_{DD} ≤ 2.9 V
I_{OL1}	Low output current on Port 0 pins	–	–	10	mA	V_{DD} ≤ 2.9 V, maximum of 20 mA sink current
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25 °C.

DC POR and LVD Specifications

Table 7. DC POR and LVD Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{PPOR0} V_{PPOR1}	V_{DD} Value for PPOR Trip V_{DD} = 2.7 V V_{DD} = 3.3 V, 5 V	– –	2.36 2.60	2.40 2.65	V V	V_{DD} must be greater than or equal to 2.5 V during startup or reset from watchdog.

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DC Flash Write Specifications

Table 8 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C < T_A < 85 °C, 3.10 V to 3.6 V and –40 °C < T_A < 85 °C or 2.4 V to 2.90 V and –40 °C < T_A < 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only. Flash Endurance and Retention specifications are valid only within the range: 25 °C ± 20 °C during the flash write operation. It is at the user's own risk to operate out of this temperature range. If flash writing is done out of this temperature range, the endurance and data retention reduces.

Table 8. DC Flash Write Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{DDIWRITE}$	Supply Voltage for Flash Write Operations[10]	2.7	–	–	V	–
I_{DDP}	Supply Current for Flash Write Operations	–	5	25	mA	–
$Flash_{ENPB}$	Flash Endurance	50,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	–

DC I^2C Specifications

This table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C < T_A < 85 °C, 3.10 V to 3.6 V and –40 °C < T_A < 85 °C or 2.4 V to 2.90 V and –40 °C < T_A < 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 9. DC I^2C Specifications

Symbol [11]	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	$0.3 \times V_{DD}$	V	$2.4\ V \le V_{DD} \le 3.6\ V$
		–	–	$0.25 \times V_{DD}$	V	$4.75\ V \le V_{DD} \le 5.25\ V$
V_{IHI2C}	Input high level	$0.7 \times V_{DD}$	–	–	V	$2.4\ V \le V_{DD} \le 5.25\ V$
V_{OLP}	Low output voltage	–	–	0.4	V	I_{OL} = 5 mA/pin, maximum of 10 mA device sink current $2.4 \le V_{DD} \le 2.9$ V and $3.1 \le V_{DD} \le 3.6$ V.
C_{I2C}	Capacitive load on I^2C pins	0.5	1.7	5	pF	Package and pin dependent. Temp = 25 °C.
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	–

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Note
10. Commands involving flash writes (0x01, 0x02, 0x03) and flash read (0x04) must be executed only within the same V_{CC} voltage range detected at POR (power on, or command 0x06) and above 2.7 V.
11. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the above specs.

CapSense Electrical Characteristics

Max (V)	Typ (V)	Min (V)	Conditions for Supply Voltage	Result
3.6	3.3	3.1	< 2.9	The device automatically reconfigures itself to work in 2.7 V mode of operation.
			> 2.9 or < 3.10	This range is not recommended for CapSense usage.
2.90	2.7	2.45	< 2.45 V	The scanning for CapSense parameters shuts down until the voltage returns to over 2.45 V.
			> 3.10	The device automatically reconfigures itself to work in 3.3 V mode of operation.
			< 2.4 V	The device goes into reset.
5.25	5.0	4.75	< 4.73 V	The scanning for CapSense parameters shuts down until the voltage returns to over 4.73 V.

AC Electrical Specifications

AC Chip-Level Specifications

Table 10. 5-V and 3.3-V AC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Units	Notes
F_{32K1}	Internal low-speed oscillator (ILO) frequency	15	32	64	kHz	Calculations during sleep operations are done based on ILO frequency.
t_{XRST}	External reset pulse width	10	–	–	µs	–
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	150	–	ms	–
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	–

Table 11. 2.7-V AC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Units	Notes
F_{32K1}	Internal low-speed oscillator (ILO) frequency	8	32	96	kHz	Calculations during sleep operations are done based on ILO frequency.
t_{XRST}	External reset pulse width	10	–	–	µs	–
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	600	–	ms	–
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	–

AC GPIO Specifications

Table 12. 5-V and 3.3-V AC GPIO Specifications

Parameter	Description	Min	Max	Unit	Notes
t_{Rise}	Rise time, strong mode, Cload = 50 pF	15	80	ns	V_{DD} = 3.10 V to 3.6 V and 4.75 V to 5.25 V, 10% to 90%
t_{Fall}	Fall time, strong mode, Cload = 50 pF	10	50	ns	V_{DD} = 3.10 V to 3.6 V and 4.75 V to 5.25 V, 10% to 90%

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Table 13. 2.7-V AC GPIO Specifications

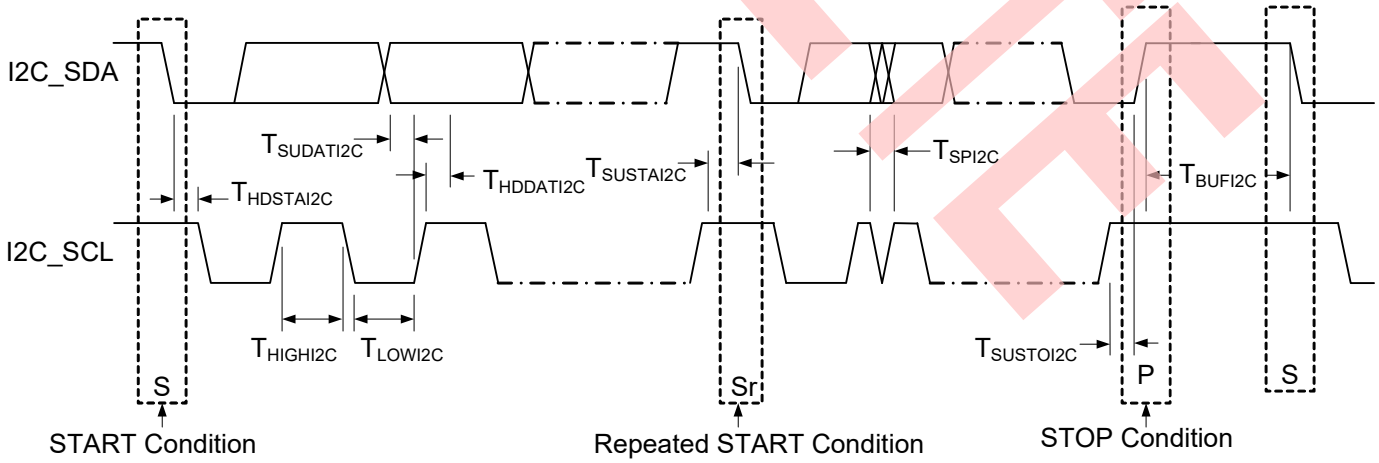
Parameter	Description	Min	Max	Unit	Notes
t_{Rise}	Rise time, strong mode, Cload = 50 pF	15	100	ns	V_{DD} = 2.4 V to 2.90 V, 10% to 90%
t_{Fall}	Fall time, strong mode, Cload = 50 pF	10	70	ns	V_{DD} = 2.4 V to 2.90 V, 10% to 90%

AC I²C Specifications

Table 14. AC I²C Specifications

Parameter	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kbps	Fast mode not supported for V_{DD} < 3.0 V
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs	–
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs	–
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	–
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	–
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs	–
$t_{SUDATI2C}$	Data setup time	250	–	100	–	ns	–
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	–
t_{BUFI2C}	BUS free time between a STOP and START condition	4.7	–	1.3	–	µs	–
t_{SPI2C}	Pulse width of spikes suppressed by the input filter	–	–	0	50	ns	–

Figure 10. Definition of Timing for Fast/Standard Mode on the I²C Bus



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Appendix

Examples of Frequently Used I²C Commands

Sl. No.	Requirement	I²C Commands[12]	Comments
1	Enter into setup mode	W 00 A0 08	–
2	Enter into normal mode	W 00 A0 07	–
3	Load factory defaults to RAM registers	W 00 A0 02	–
4	Do a software reset	W 00 A0 08 W 00 A0 06	; Enter into setup mode ; Do software reset
5	Save current configuration to flash	W 00 A0 01	–
6	Load factory defaults to RAM registers and save as user configuration	W 00 A0 08 W 00 A0 02 W 00 A0 01 W 00 A0 06	; Enter into setup mode ; Load factory defaults to SRAM ; Save the configuration to flash. Wait for time specified in CapSense Express Commands on page 12. ; Do software reset
7	Disable combinational logic output to DIG0	W 00 1C 00	–
8	Disable combinational logic output to DIG1	W 00 21 00	–
9	Clearing (logic 0) the both DIG0 and DIG1 outputs	W 00 04 00	Combinational logic output on DIG0 and DIG1 should be disabled before dong this operation (SL# 7 and 8)
10	Setting (logic 1) the DIG0 and clearing (Logic 0) the DIG1 outputs	W 00 04 01	–
11	Clearing (logic 0) the DIG0 and Setting (Logic 1) the DIG1 outputs	W 00 04 02	–
12	Setting (logic 1) the both DIG0 and DIG1 outputs	W 00 04 03	–
13	Change CapSense clock to IMO/2	W 00 A0 08 W 00 51 20 W 00 A0 07	; Enter into setup mode ; CapSense clock is set as IMO/2 ; Enter into normal mode
14	Change value of IDAC0 to ‘x’h	W 00 70 x	‘x’ represents new value of IDAC register
15	Change value of IDAC1 to ‘y’h	W 00 71 y	‘y’ represents new value of IDAC register
16	Change value of IDAC0 and IDAC1 to ‘x’h and ‘y’h	W 00 70 x y	‘x’ and ‘y’ represents new value of IDAC register
17	Change the value FT0 to ‘x’h	W 00 66 x	‘x’ represents new value of FT register
18	Change the value FT1 to ‘y’h	W 00 67 y	‘y’ represents new value of FT register
19	Change the value FT0 and FT1 to ‘x’h and ‘y’h	W 00 66 x y	‘x’ and ‘y’ represents new value of FT registers
20	Change noise threshold to ‘x’h	W 00 4E x	–
21	Read CapSense button CS0 scan results	W 00 81 81 W 00 82 R 00 RD RD RD RD RD RD	; Select CapSense button for reading scan result ; Set the read point to 82h ; Consecutive 6 reads gets baseline, difference count and raw count (all two byte each)
22	Read CapSense button status register	W 00 88 R 00 RD	; Set the read pointer to 88 ; Reading a byte gets status CapSense inputs

Note
12. The ‘W’ indicates the write transfer and the next byte of data represents the 7-bit I2C address. The I2C address is assumed to be ‘0’ in the above examples. Similarly ‘R’ indicates the read transfer followed by 7-bit address and data byte read operations.

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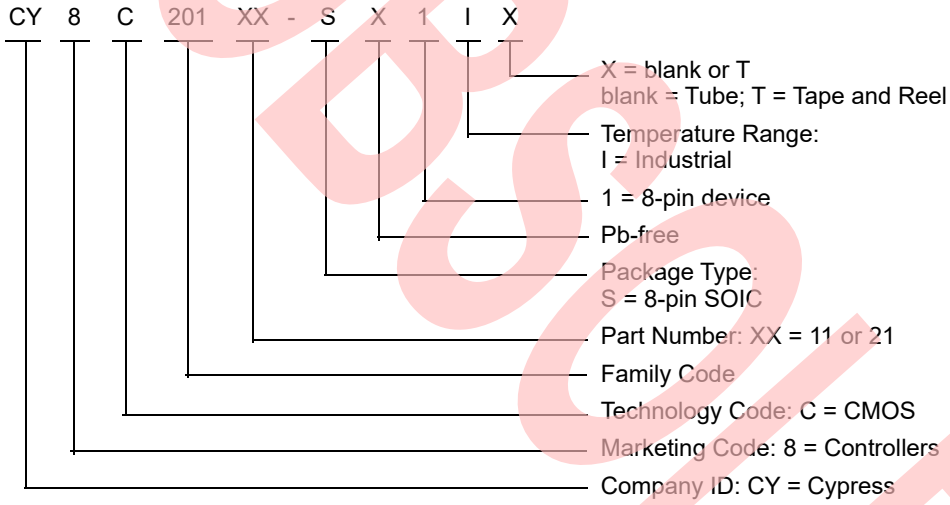
Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Temperature	CapSense Blocks	CapSense Inputs	Digital Outputs	XRES Pin
CY8C20111-SX1I	51-85066	8-pin SOIC	Industrial	Yes	1	1	No
CY8C20111-SX1IT	51-85066	8-pin SOIC (Tape and Reel)	Industrial	Yes	1	1	No
CY8C20121-SX1I	51-85066	8-pin SOIC	Industrial	Yes	2	2	No
CY8C20121-SX1IT	51-85066	8-pin SOIC (Tape and Reel)	Industrial	Yes	2	2	No

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions



Thermal Impedances

Table 15. Thermal Impedance by Package

Package	Typical θ_{JA} [13]
8-pin SOIC	127.22 °C/W

Solder Reflow Specifications

Table 16. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
8-pin SOIC	260 °C	30 seconds

Note
13. $T_J = T_A + \text{Power} \times \theta_{JA}$.

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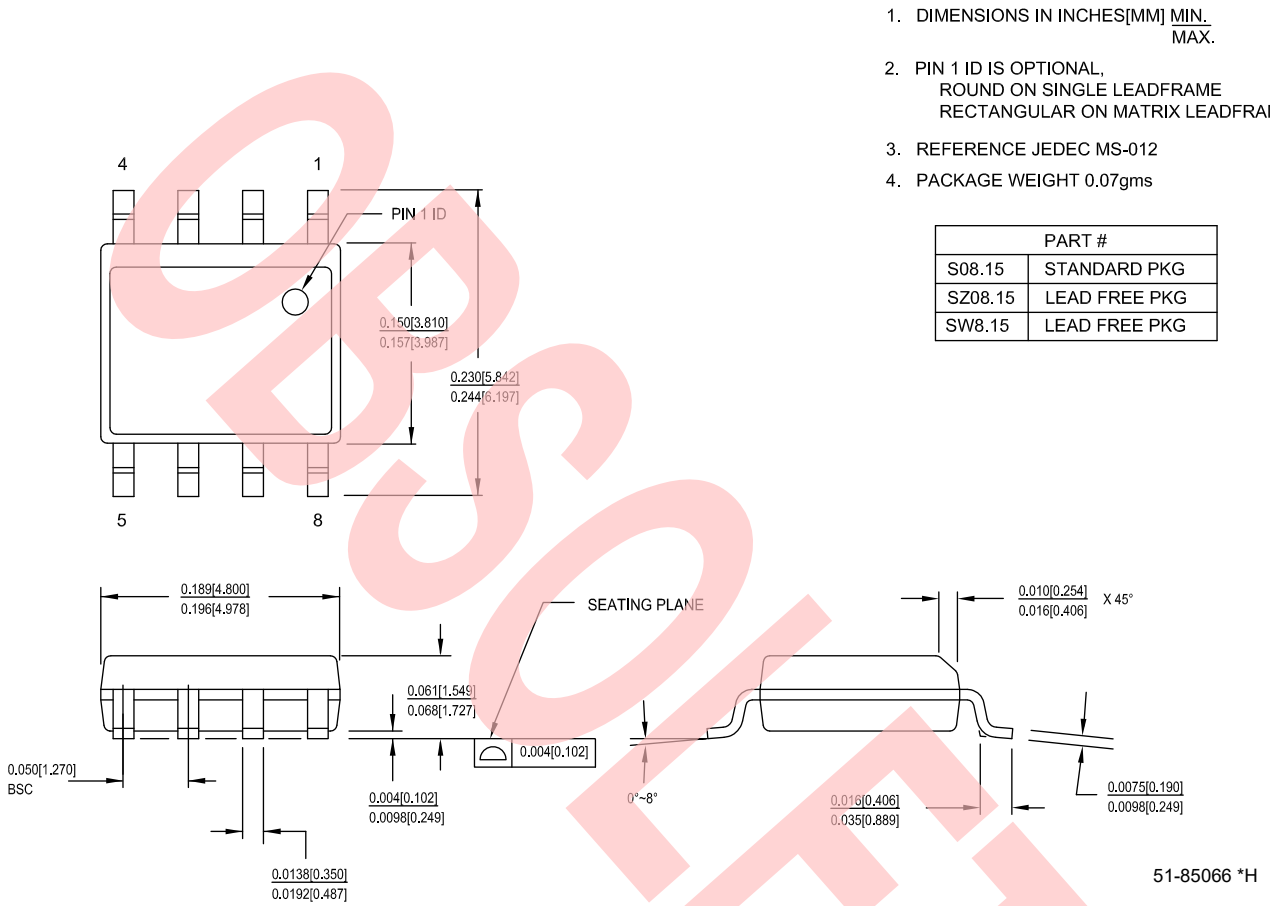
Package Diagram

Figure 11. 8-pin SOIC (150 Mils) S08.15/SZ08.15 Package Outline, 51-85066



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Acronyms

Table 17. Acronyms Used in this Document

Acronym	Description	Acronym	Description
AC	alternating current	LVD	low voltage detect
CMOS	complementary metal oxide semiconductor	PCB	printed circuit board
CRC	cyclic redundancy check	PGA	programmable gain amplifier
CSA	capsense successive approximation	POR	power on reset
CSD	capsense sigma delta	PPOR	precision power on reset
DC	direct current	PSoC®	programmable system-on-chip
EEPROM	electrically erasable programmable read-only memory	PWM	pulse width modulator
EMC	electromagnetic compatibility	QFN	quad flat no leads
GPIO	general-purpose I/O	SLIMO	slow internal main oscillator
I/O	input/output	SPITM	serial peripheral interface
IDAC	current DAC	SRAM	static random access memory
ILO	internal low speed oscillator	SROM	supervisory read only memory
IMO	internal main oscillator	SSOP	shrink small-outline package
LCD	liquid crystal display	USB	universal serial bus
LDO	low dropout regulator	WDT	watchdog timer
LED	light-emitting diode	WLCSP	wafer level chip scale package
LSB	least-significant bit	XRES	external reset

Document Conventions

Units of Measure

Table 18. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	mm	millimeter
kbps	kilo bits per second	ms	millisecond
kHz	kilohertz	nA	nanoampere
kΩ	kilohm	ns	nanosecond
LSB	least significant bit	%	percent
µA	microampere	pF	picofarad
µs	microsecond	V	volt
mA	milliampere	W	watt

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

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Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for I/O operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.

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Glossary *(continued)*

cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.

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Glossary *(continued)*

low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device***.
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and I/O circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
Phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
Power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is a type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.

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Glossary *(continued)*

settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

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Errata

CY8C20111/121

This section describes the errata for the CapSense Express devices, CY8C20111/121. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Package Type	Operating Range
CY8C20111	All packages	Industrial
CY8C20121	All packages	Industrial

Product Status

The CY8C20111/121 CapSense Express devices have been qualified and are available in production quantities.

CapSense Express CY8C20111/121 Errata Summary

Table 19 defines the errata applicable to CY8C20111/121 Cypress CapSense Express devices.

Table 19. CapSense Express CY8C20110 Errata Summary

Item	Issues/Changes	Description	Fix Status
1	False triggering during power-up	If a finger is on the sensor during power-up, the sensor triggers and the baseline gets stuck. This occurs only when the Averaging Filter is enabled.	No fix will be provided. Disable the AveragingFilter if your design requires a finger on the sensor during power-up.
2	Erroneous I2C START condition detection	During boot up, CapSense Express device misinterprets an incoming byte as its own address leading to confusion in the I2C state machine. It controls the SCL and SDA line in between the I2C transfer leading to bus communication failure.	No fix will be provided. Do not initiate I2C transactions on bus before the device boots up.

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Document History Page

Document Title: CY8C20111/CY8C20121, CapSense® Express™ – One Button and Two Button Capacitive Controllers Document Number: 001-53516				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2709248	SLAN / PYRS	See ECN	New datasheet.
*A	2821828	SSHH / FSU	12/4/2009	Added Contents. Updated Registers (Updated Register Map, added OUTPUT_STATUS). Updated Absolute Maximum Ratings (Added F32k u, $t_{POWERUP}$ parameters and their details). Updated Electrical Specifications (Updated DC Electrical Specifications (Updated DC Flash Write Specifications (Updated Note 10))).
*B	2868929	SLAN	01/28/2010	Changed status from Preliminary to Final. Updated Package Diagram (spec 51-85066 (Changed revision from *C to *D)).
*C	2892629	NJF	03/15/2010	Updated Absolute Maximum Ratings (Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters and their details). Added Thermal Impedances. Added Solder Reflow Specifications.
*D	3043236	ARVM	09/30/2010	Updated Absolute Maximum Ratings (Removed F32ku, $t_{POWERUP}$ parameters and their details). Updated Electrical Specifications (Updated AC Electrical Specifications (Added AC Chip-Level Specifications)).
*E	3087790	NJF	11/16/2010	Updated Electrical Specifications ((Updated DC Electrical Specifications (Updated DC GPIO Specifications (Removed sub-section “2.7-V DC Spec for I^2C Line with 1.8 V External Pull-up”), added DC I2C Specifications)), updated AC Electrical Specifications (Updated AC I^2C Specifications (Updated Figure 10 (No specific changes were made to I2C Timing Diagram. Updated for clearer understanding.)))). Updated Solder Reflow Specifications. Added Acronyms and Units of Measure. Added Glossary. Updated in new template.
*F	3148656	ARVM	01/20/2011	Updated Layout Guidelines and Best Practices (Updated Table 3 (Removed “Overlay thickness-buttons” category), added the following statement after Table 3 – “The Recommended maximum overlay thickness is 2 mm. For more details refer to the section “The Integrating Capacitor (Cint)” in AN53490.”). Updated CapSense Constraints (Removed the parameter “Overlay thickness”). Updated Solder Reflow Specifications (Updated Table 16).
*G	3287607	ARVM	06/20/2011	Post to external web.
*H	3631370	VAIR / SLAN	05/31/2012	Updated Typical Circuits (Updated Figure 6 (Added Note 3 and referred the same Note in Figure 6)). Updated in new template.
*I	3759474	PRIA	09/28/2012	Corrected following typos: 1. Incorrect reference, updated reference to Table 1 in Page 8. 2. In Page 22, CS_READ_BUTTON register, changed I2C_ADDR_DM: 81h to CS_READ_BUTTON: 81h.

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Document History Page *(continued)*

Document Title: CY8C20111/CY8C20121, CapSense® Express™ – One Button and Two Button Capacitive Controllers Document Number: 001-53516				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*J	4402835	PRIA	06/09/2014	Updated Registers: Updated CS_READ_DIFFx: Updated register addresses of CS_READ_DIFFM and CS_READ_DIFFL. Updated CS_READ_RAWx: Updated register addresses of CS_READ_RAWM and CS_READ_RAWL. Updated Package Diagram: spec 51-85066 – Changed revision from *E to *F. Updated in new template. Completing Sunset Review.
*K	4812735	PRIA	06/26/2015	Added a note on Errata in page 1. Updated I2C Clock Stretching, Layout Guidelines and Best Practices. Removed Figure 10 through Figure 14. Added Errata. Updated Figure 11 in Package Diagram (spec 51-85066 *F to *G).
*L	4906712	PRIA	09/03/2015	Fixing formatting updates to the document.
*M	5277446	PRIA	05/19/2016	Added “Not recommended for new designs” watermark. Updated the template.
*N	6015630	PRIA	01/05/2018	Obsolete this document, as it is not recommended for new design.

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