18-Channel GAMMA VOLTAGE GENERATOR with Two Programmable \( V_{\text{COM}} \) Channels

**FEATURES**
- 18-CHANNEL GAMMA CORRECTION
- 2-CHANNEL PROGRAMMABLE \( V_{\text{COM}} \): 100mA \( I_{\text{OUT}} \)
- ON-CHIP OTP MEMORY
- 10-BIT RESOLUTION
- RAIL-TO-RAIL OUTPUT
- LOW SUPPLY CURRENT: 900\( \mu \)A/ch
- SUPPLY VOLTAGE: 7V to 18V
- DIGITAL SUPPLY: 2.0V to 5.5V
- INDUSTRY-STANDARD, TWO-WIRE INTERFACE: 3.4MHz HIGH-SPEED MODE
- HIGH ESD RATING: 4kV HBM, 1kV CDM, 200V MM
- DEMO BOARD AND SOFTWARE AVAILABLE

**APPLICATIONS**
- REPLACES RESISTOR-BASED GAMMA SOLUTIONS
- TFT-LCD REFERENCE DRIVERS
- DYNAMIC GAMMA CONTROL

**DESCRIPTION**

The BUF20820 is a programmable voltage reference generator designed for gamma correction in TFT-LCD panels. It provides 18 programmable outputs for gamma correction and two channels for \( V_{\text{COM}} \) adjustment, each with 10-bit resolution. It offers on-chip One-Time Programmable (OTP) memory that allows the user to store the gamma voltages on-chip. This eliminates the need for an external EEPROM.

This programmability replaces the traditional, time-consuming process of changing resistor values to optimize the various gamma voltages and allows designers to determine the correct gamma voltages for a panel very quickly. Required voltage changes can also be easily implemented without hardware changes.

The BUF20820 uses TI's latest, small-geometry analog CMOS process, which makes it a very competitive choice for full production, not just evaluation.

Programming of each output occurs through an industry-standard, two-wire serial interface. Unlike existing programmable buffers, the BUF20820 offers a high-speed mode that allows clock speeds up to 3.4MHz.

For lower or higher channel count, please contact your local sales or marketing representative.

The BUF20820 is available in an HTSSOP-38 PowerPAD™ package. It is specified from \(-40^\circ C\) to \(+85^\circ C\).

**BUF20820 RELATED PRODUCTS**

<table>
<thead>
<tr>
<th>FEATURES</th>
<th>PRODUCT</th>
</tr>
</thead>
<tbody>
<tr>
<td>18-Channel Programmable, Two ( V_{\text{COM}} )</td>
<td>BUF20800</td>
</tr>
<tr>
<td>12-Channel Programmable Buffer, 10-Bit</td>
<td>BUF12800</td>
</tr>
<tr>
<td>Programmable ( V_{\text{COM}} ) with Memory</td>
<td>BUF01900</td>
</tr>
<tr>
<td>10-Channel Gamma Correction Buffer, Int ( V_{\text{COM}} )</td>
<td>BUF11704</td>
</tr>
<tr>
<td>18V Operating Supply Voltage</td>
<td>SN10501</td>
</tr>
<tr>
<td>High-Speed ( V_{\text{COM}} ), 1 and 2 Channels</td>
<td>TPS651xx</td>
</tr>
<tr>
<td>Complete LCD DC/DC Solution</td>
<td></td>
</tr>
</tbody>
</table>

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a registered trademark of Texas Instruments. All other trademarks are the property of their respective owners.
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, $V_S$</td>
<td>$+19V$</td>
</tr>
<tr>
<td>Supply Voltage, $V_{SD}$</td>
<td>$+6V$</td>
</tr>
<tr>
<td>Signal Input Terminals, SCL, SDA, AO, LD:</td>
<td></td>
</tr>
<tr>
<td>Voltage</td>
<td>$-0.5V$ to $+6V$</td>
</tr>
<tr>
<td>Current</td>
<td>$\pm10mA$</td>
</tr>
<tr>
<td>Output Short Circuit</td>
<td>Continuous</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>$-40^\circ C$ to $+95^\circ C$</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>$-65^\circ C$ to $+150^\circ C$</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>$+125^\circ C$</td>
</tr>
<tr>
<td>ESD Rating:</td>
<td></td>
</tr>
<tr>
<td>Human Body Model (HBM)</td>
<td>$4kV$</td>
</tr>
<tr>
<td>Charged-Device Model (CDM)</td>
<td>$1kV$</td>
</tr>
<tr>
<td>Machine Model (MM)</td>
<td>$200V$</td>
</tr>
</tbody>
</table>

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Short-circuit to ground.

**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>PACKAGE-LEAD</th>
<th>PACKAGE DESIGNATOR</th>
<th>PACKAGE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>BUF20820</td>
<td>HTSSOP-38</td>
<td>DCP</td>
<td>BUF20820</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, $T_A = -40^\circ C$ to $+85^\circ C$.

At $T_A = +25^\circ C$, $V_S = 18V$, $V_{SD} = 5V$, $V_{REFH} = 17V$, $V_{REFL} = 1V$, $R_L = 1.5k\Omega$ connected to ground, and $C_L = 200pF$, unless otherwise noted.

### Analog Power Supply

<table>
<thead>
<tr>
<th>Condition</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_S$ No Load</td>
<td>$15$</td>
<td>$18$</td>
<td>$28$</td>
<td>mA</td>
</tr>
<tr>
<td>$I_S$ No Load</td>
<td>$25$</td>
<td>$50$</td>
<td>$100$</td>
<td>µA</td>
</tr>
</tbody>
</table>

### Voltage Levels

- $V_{IH} = 0.7 \times V_{SD}$
- $V_{IL} = 0.3 \times V_{SD}$

### Digital Power Supply

<table>
<thead>
<tr>
<th>Condition</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{SD}$ No-Load, Two-Wire Bus Inactive</td>
<td>$2.0$</td>
<td>$5.5$</td>
<td>$100$</td>
</tr>
</tbody>
</table>

### Temperature

<table>
<thead>
<tr>
<th>Condition</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\theta_J$ Junction-to-Ambient</td>
<td>$30$</td>
<td>$+85$</td>
<td>$\degree C/W$</td>
</tr>
<tr>
<td>$\theta_C$ Junction-to-Case</td>
<td>$15$</td>
<td>$+95$</td>
<td>$\degree C/W$</td>
</tr>
</tbody>
</table>
## PIN CONFIGURATIONS

### Top View

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>$V_{\text{COM OUt 2}}$</td>
</tr>
<tr>
<td>2</td>
<td>REFH</td>
</tr>
<tr>
<td>3</td>
<td>NC$^{(1)}$</td>
</tr>
<tr>
<td>4</td>
<td>NC$^{(1)}$</td>
</tr>
<tr>
<td>5</td>
<td>OUT1</td>
</tr>
<tr>
<td>6</td>
<td>OUT2</td>
</tr>
<tr>
<td>7</td>
<td>OUT3</td>
</tr>
<tr>
<td>8</td>
<td>OUT4</td>
</tr>
<tr>
<td>9</td>
<td>OUT5</td>
</tr>
<tr>
<td>10</td>
<td>OUT6</td>
</tr>
<tr>
<td>11</td>
<td>$V_S^\text{A}$</td>
</tr>
<tr>
<td>12</td>
<td>$V_S^\text{A}$</td>
</tr>
<tr>
<td>13</td>
<td>OUT7</td>
</tr>
<tr>
<td>14</td>
<td>OUT8</td>
</tr>
<tr>
<td>15</td>
<td>OUT9</td>
</tr>
<tr>
<td>16</td>
<td>REFH OUT</td>
</tr>
<tr>
<td>17</td>
<td>$V_{SD}$</td>
</tr>
<tr>
<td>18</td>
<td>SCL</td>
</tr>
<tr>
<td>19</td>
<td>SDA</td>
</tr>
<tr>
<td>20</td>
<td>AO</td>
</tr>
<tr>
<td>31</td>
<td>OUT16</td>
</tr>
<tr>
<td>32</td>
<td>OUT17</td>
</tr>
<tr>
<td>33</td>
<td>OUT18</td>
</tr>
<tr>
<td>34</td>
<td>REFH OUT</td>
</tr>
<tr>
<td>35</td>
<td>NC$^{(1)}$</td>
</tr>
<tr>
<td>36</td>
<td>NC$^{(1)}$</td>
</tr>
<tr>
<td>37</td>
<td>REFL</td>
</tr>
<tr>
<td>38</td>
<td>$V_{\text{COM OUT 1}}$</td>
</tr>
</tbody>
</table>

### HTSSOP

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$V_{\text{COM OUt 2}}$</td>
</tr>
<tr>
<td>2</td>
<td>REFH</td>
</tr>
<tr>
<td>3</td>
<td>NC$^{(1)}$</td>
</tr>
<tr>
<td>4</td>
<td>NC$^{(1)}$</td>
</tr>
<tr>
<td>5</td>
<td>OUT1</td>
</tr>
<tr>
<td>6</td>
<td>OUT2</td>
</tr>
<tr>
<td>7</td>
<td>OUT3</td>
</tr>
<tr>
<td>8</td>
<td>OUT4</td>
</tr>
<tr>
<td>9</td>
<td>OUT5</td>
</tr>
<tr>
<td>10</td>
<td>OUT6</td>
</tr>
<tr>
<td>11</td>
<td>$V_S^\text{A}$</td>
</tr>
<tr>
<td>12</td>
<td>$V_S^\text{A}$</td>
</tr>
<tr>
<td>13</td>
<td>OUT7</td>
</tr>
<tr>
<td>14</td>
<td>OUT8</td>
</tr>
<tr>
<td>15</td>
<td>OUT9</td>
</tr>
<tr>
<td>16</td>
<td>REFH OUT</td>
</tr>
<tr>
<td>17</td>
<td>$V_{SD}$</td>
</tr>
<tr>
<td>18</td>
<td>SCL</td>
</tr>
<tr>
<td>19</td>
<td>SDA</td>
</tr>
<tr>
<td>20</td>
<td>AO</td>
</tr>
<tr>
<td>21</td>
<td>LD</td>
</tr>
<tr>
<td>22</td>
<td>GND$^\text{D}$</td>
</tr>
<tr>
<td>23</td>
<td>OUT10</td>
</tr>
<tr>
<td>24</td>
<td>OUT11</td>
</tr>
<tr>
<td>25</td>
<td>OUT12</td>
</tr>
<tr>
<td>26</td>
<td>OUT13</td>
</tr>
<tr>
<td>27</td>
<td>$V_S^\text{B}$</td>
</tr>
<tr>
<td>28</td>
<td>GND$^\text{A}$</td>
</tr>
<tr>
<td>29</td>
<td>OUT14</td>
</tr>
<tr>
<td>30</td>
<td>OUT15</td>
</tr>
<tr>
<td>31</td>
<td>OUT16</td>
</tr>
<tr>
<td>32</td>
<td>OUT17</td>
</tr>
<tr>
<td>33</td>
<td>OUT18</td>
</tr>
</tbody>
</table>

---

(1) NC denotes no connection.

(2) GND$_D$ and GND$_A$ are internally connected and must be at the same voltage potential.
TYPICAL CHARACTERISTICS
At $T_A = +25\, ^\circ\text{C}$, $V_S = 18\text{V}$, $V_{SD} = 5\text{V}$, $V_{REFH} = 17\text{V}$, $V_{REFL} = 1\text{V}$, $R_L = 1.5k\Omega$ connected to ground, and $C_L = 200\text{pF}$, unless otherwise noted.
APPLICATIONS INFORMATION

The BUF20820 programmable voltage reference allows fast and easy adjustment of 18 programmable reference outputs and two channels for VCOM adjustment, each with 10-bit resolution. It allows very simple, time-efficient adjustment of the gamma reference and VCOM voltages. The BUF20820 is programmed through a high-speed, standard, two-wire interface. The BUF20820 features a double-register structure for each DAC channel to simplify the implementation of dynamic gamma control. This design allows pre-loading of register data and rapid updating of all channels simultaneously.

Buffers 1–9 are able to swing to within 200mV of the positive supply rail, and to within 0.6V of the negative supply rail. Buffers 10–18 are able to swing to within 0.8V of the positive supply rail and to within 200mV of the negative supply rail.

The BUF20820 can be powered using an analog supply voltage from 7V to 18V, and a digital supply from 2V to 5.5V. The digital supply must be applied prior to or simultaneously with the analog supply to avoid excessive current and power consumption; damage to the device may occur if it is left connected only to the analog supply for extended periods of time. Figure 7 shows the power supply timing requirements.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to a LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the 9th clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent followed by an Acknowledge Bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH will be interpreted as a START or STOP condition.

Once all data have been transferred, the master generates a STOP condition indicated by pulling SDA from LOW to HIGH while SCL is HIGH.

The BUF20820 can act only as a slave device; therefore, it never drives SCL. SCL is only an input for the BUF20820. Table 1 and Table 2 summarize the address and command codes, respectively, for the BUF20820.

ADDRESSING THE BUF20820

The address of the BUF20820 is 111010x, where x is the state of the A0 pin. When the A0 pin is LOW, the device will acknowledge on address 74h (1110100). If the A0 pin is HIGH, the device will acknowledge on address 75h (1110101).

Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

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Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

Table 1. Quick-Reference Table of BUF20820 Addresses

<table>
<thead>
<tr>
<th>DEVICE/COMPONENT</th>
<th>ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>BUF20820 Address:</td>
<td></td>
</tr>
<tr>
<td>A0 pin is LOW</td>
<td>1110100</td>
</tr>
<tr>
<td>(device will acknowledge on address 74h)</td>
<td></td>
</tr>
<tr>
<td>A0 pin is HIGH</td>
<td>1110101</td>
</tr>
<tr>
<td>(device will acknowledge on address 75h)</td>
<td></td>
</tr>
</tbody>
</table>

Table 2. Quick-Reference Table of Command Codes

<table>
<thead>
<tr>
<th>COMMAND</th>
<th>CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>General Call Reset</td>
<td>Address byte of 00h followed by a data byte of 06h.</td>
</tr>
<tr>
<td>High-Speed Mode</td>
<td>00001xxx, with SCL ≤ 400kHz; where xxx are bits unique to the Hs-capable master. This byte is called the Hs master code.</td>
</tr>
</tbody>
</table>
Figure 8. Typical Application Configuration

NOTES: (1) RC combination optional.
(2) Connecting a capacitor to this node is not recommended.
(3) GND_A and GND_D must be connected together.
(4) Pins 12 and 27 are V_S. The one set of capacitors shown on pin 27 are common to both pins.
DATA RATES
The two-wire bus operates in one of three speed modes:
- Standard: allows a clock frequency of up to 100kHz;
- Fast: allows a clock frequency of up to 400kHz; and
- High-speed mode (or Hs mode): allows a clock frequency of up to 3.4MHz.

The BUF20820 is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00011xxx, with SCL = 400kHz, following the START condition; xxx are bits unique to the Hs-capable master, which can be any value. This byte is called the Hs master code. (Note that this is different from normal address bytes—the low bit does not indicate read/write status.) The BUF20820 will respond to the High-speed command regardless of the value of these last three bits. The BUF20820 will not acknowledge this byte; the communication protocol prohibits acknowledgement of the Hs master code. On receiving a master code, the BUF20820 will switch on its Hs mode filters, and communicate at up to 3.4MHz. Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat START without a STOP. The BUF20820 will switch out of Hs mode with the next STOP condition.

GENERAL CALL RESET AND POWER-UP
The BUF20820 responds to a General Call Reset, which is an address byte of 00h (0000 0000) followed by a data byte of 06h (0000 0110). The BUF20820 acknowledges both bytes. Upon receiving a General Call Reset, the BUF20820 performs a full internal reset, as though it had been powered off and then on. It always acknowledges the General Call address byte of 00h (0000 0000), but does not acknowledge any General Call data bytes other than 06h (0000 0110).

The BUF20820 automatically performs a reset upon power-up. As part of the reset, the BUF20820 is configured for all outputs to change to the programmed OTP memory values, or to ‘0000’ if the OTP values have not been programmed.

The BUF20820 resets all outputs to the OTP memory values (or to ‘0000’ if the OTP values have not been programmed) when the device address is sent, followed by a valid DAC address with bits D7 to D5 set to ‘100’. If these bits are set to ‘010’, only the DAC being addressed will be reset.

OUTPUT VOLTAGE
Buffer output values are determined by the reference voltages \( V_{\text{REFH}} \) and \( V_{\text{REFL}} \) and the decimal value of the binary input code used to program that buffer. The value is calculated using Equation 1:

\[
V_{\text{OUT}} = \left[ \frac{V_{\text{REFH}} - V_{\text{REFL}}}{1024} \times \text{Decimal Value of Code} \right] + V_{\text{REFL}}
\]

The valid voltage ranges for the reference voltages are:

\[
4V \leq V_{\text{REFH}} \leq V_{\text{S}} - 0.2V \quad \text{and} \quad 0.2V \leq V_{\text{REFL}} \leq V_{\text{S}} - 4V
\]

The BUF20820 outputs are capable of a full-scale voltage output change in typically 5\(\mu\)s—no intermediate steps are required.

OUTPUT LATCH
Updating the DAC register is not the same as updating the DAC output voltage, because the BUF20820 features a double-buffered register structure. There are three methods for latching transferred data from the storage registers into the DACs to update the DAC output voltages.

Method 1 requires externally setting the latch pin (LD) LOW, LD = LOW, which will update each DAC output voltage whenever its corresponding register is updated.

Method 2 externally sets LD = HIGH to allow all DAC output voltages to retain their values during data transfer and until LD = LOW, which will then simultaneously update the output voltages of all DACs to the new register values. Use this method to transfer a future data set in advance to prepare for a very fast output voltage update.

Method 3 uses software control. LD is maintained HIGH, and all DACs are updated when the master writes a 1 in bit 15 and a 0 in bit 14 of any DAC register. The update will occur after receiving the 16-bit data for the currently-written register.

The General Call Reset and the power-up reset will update the DAC regardless of the state of the latch pin.
ACQUIRE OF OTP MEMORY

A general acquire command will update all registers and DAC outputs to the values stored in OTP memory.

A single channel acquire command will update only the register and DAC output of the DAC corresponding to the DAC address used in the command.

General Acquire Command
1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send a DAC address byte. Bits D7–D5 must be set to 100. Bits D4–D0 are any valid DAC address. Only addresses 00000 to 10100 are valid and will be acknowledged. Table 3 shows the valid addresses.
4. Send a STOP condition on the bus.

Following this command, all DAC registers and DAC outputs will change to the OTP memory values.

Table 3. DAC Addresses

<table>
<thead>
<tr>
<th>DAC</th>
<th>ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC_1</td>
<td>0 0000</td>
</tr>
<tr>
<td>DAC_2</td>
<td>0 0001</td>
</tr>
<tr>
<td>DAC_3</td>
<td>0 0010</td>
</tr>
<tr>
<td>DAC_4</td>
<td>0 0011</td>
</tr>
<tr>
<td>DAC_5</td>
<td>0 0100</td>
</tr>
<tr>
<td>DAC_6</td>
<td>0 0101</td>
</tr>
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<td>DAC_7</td>
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<td>DAC_8</td>
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<td>DAC_18</td>
<td>1 0001</td>
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<tr>
<td>VCOM_OUT1</td>
<td>1 0010</td>
</tr>
<tr>
<td>VCOM_OUT2</td>
<td>1 0011</td>
</tr>
<tr>
<td>Write Disable Bit</td>
<td>1 0100</td>
</tr>
</tbody>
</table>

Single Channel Acquire Command
1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send a DAC address byte using the DAC address corresponding to the DAC output and register to update with the OTP memory value. Bits D7–D5 must be set to 010. Bits D4–D0 are the DAC address. Only DAC addresses 00000 to 10100 are valid and will be acknowledged. Table 3 shows the valid addresses.
4. Send a STOP condition on the bus.

See Figure 9 for the timing diagrams for the acquire commands.

READ/WRITE OPERATIONS

Single or multiple read and write operations can be done in a single communication transaction. Writing to a DAC register differs from writing to the OTP memory. Bits D15–D14 of the most significant byte of data will determine if data will be written to the DAC register or the OTP memory. See Figure 10 through Figure 12 for the timing diagrams and timing requirements for the read/write commands.

Read/Write: DAC register

The BUF20820 is able to read from a single DAC, or multiple DACs, or write to the register of a single DAC, or multiple DACs in a single communication transaction. DAC addresses begin with 00000, which corresponds to DAC_1, through 10011, which corresponds to VCOM_OUT2.

Write commands are performed by setting the read/write bit LOW. Setting the read/write bit HIGH will perform a read transaction.

Writing:
To write to a single DAC register:
1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send a DAC or write disable bit address byte. Bits D7–D5 must be set to 0. Bits D4–D0 are the DAC address. Only addresses 00000 to 10100 are valid and will be acknowledged. Table 3 shows valid addresses.
4. Send two bytes of data for the specified DAC register. Begin by sending the most significant byte first (bits D15–D8, of which only bits D9 and D8 are used, and bits D15–D14 must not be 01), followed by the least significant byte (bits D7–D0). For address 10100, only D0 has meaning. This bit is the write disable bit. The register is updated after receiving the second byte.
5. Send a STOP condition on the bus.

The BUF20820 will acknowledge each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified register will not be updated. Updating the DAC register is not the same as updating the DAC output voltage. See the Output Latch section.

The process of updating multiple DAC registers begins the same as when updating a single register. However, instead of sending a STOP condition after writing the
addressed register, the master continues to send data for the next register. The BUF20820 automatically and sequentially steps through subsequent registers as additional data is sent. The process continues until all desired registers have been updated or a STOP condition is sent.

To write to multiple DAC registers:
1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send either the DAC_1 address byte to start at the first DAC, or send the address byte for whichever DAC will be the first in the sequence of DACs to be updated. The BUF20820 will begin with this DAC and step through subsequent DACs in sequential order.
4. Send the bytes of data; begin by sending the most significant byte (bits D15–D8, of which only bits D9 and D8 have meaning, and bits D15–D14 must not be 01), followed by the least significant byte (bits D7–D0). The first two bytes are for the DAC addressed in step 3 above. Its register is automatically updated after receiving the second byte. The next two bytes are for the following DAC. That DAC register is updated after receiving the fourth byte. This process continues until the registers of all following DACs have been updated. The last address, 10100, is the address of the write disable bit and cannot be accessed using this method. It must be written using the write to a single DAC register procedure.
5. Send a STOP condition on the bus.

The BUF20820 will acknowledge each byte. To terminate communication, send a STOP or START condition on the bus. Only DAC registers that have received both bytes of data will be updated.

Reading:
Reading a DAC register will return the data stored in the DAC. This data can differ from the data stored in the DAC register. See the Output Latch section.

To read the DAC value:
1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send the DAC address byte. Bits D7–D5 must be set to 0; Bits D4–D0 are the DAC address. Only DAC addresses 00000 to 10100 are valid and will be acknowledged. For address 10100, only D0 has meaning. This bit is the write disable bit.
4. Send a START or STOP/START condition on the bus.

5. Send correct device address and read/write bit = HIGH. The BUF20820 will acknowledge this byte.
6. Receive two bytes of data. They are for the specified DAC. The first received byte is the most significant byte (bits D15–D8, only bits D9 and D8 have meaning); the next byte is the least significant byte (bits D7–D0).
7. Acknowledge after receiving the first byte.
8. Do not acknowledge the second byte to end the read transaction.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge.

To Read Multiple DACs:
1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send either the DAC_1 address byte to start at the first DAC, or send the address byte for whichever DAC will be the first in the sequence of DACs to be read. The BUF20820 will begin with this DAC and step through subsequent DACs in sequential order.
4. Send a START or STOP/START condition on the bus.
5. Send correct device address and read/write bit = HIGH. The BUF20820 will acknowledge this byte.
6. Receive two bytes of data. They are for the specified DAC. The first received byte is the most significant byte (bits D15–D8, only bits D9 and D8 have meaning), the next byte is the least significant byte (bits D7–D0).
7. Acknowledge after receiving each byte of data except for the last byte. The acknowledge bit of the last byte should be HIGH to end the read operation.
8. When all desired DACs have been read, send a STOP or START condition on the bus.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge.
Write: OTP Memory for the DAC Register

The BUF20820 is able to write to the OTP memory of a single DAC, or multiple DACs in a single communication transaction. DAC addresses begin with 00000 (which corresponds to DAC_1) through 10011 (which corresponds to $V_{COM\,OUT2}$).

When programming the OTP memory, the analog supply voltage must be between 8.5V and 18V.

Write commands are performed by setting the read/write bit LOW.

To write to a single OTP register:
1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send a DAC address byte. Bits D7−D5 must be set to 0. Bits D4−D0 are the DAC address. Only DAC addresses 00000 to 10100 are valid and will be acknowledged. See Table 3 for DAC addresses.
4. Send two bytes of data for the OTP register of the specified DAC. Begin by sending the most significant byte first (bits D15−D8, of which only bits D9 and D8 have meaning, and bits D15−D14 must be 01), followed by the least significant byte (bits D7−D0). For address 10100, only D0 has meaning. This bit is the write disable bit. The register is updated after receiving the second byte.
5. Send a STOP condition on the bus.

The BUF20820 will acknowledge each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified OTP register will not be updated. Writing an OTP register will also update the DAC register and output voltage.

To write to multiple OTP registers:
1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send either the DAC_1 address byte to start at the OTP register of the first DAC, or send the address byte for whichever DAC will be the first in the sequence to be updated. The BUF20820 will begin with the OTP register of this DAC and step through subsequent registers in sequential order.
4. Send the bytes of data; begin by sending the most significant byte (bits D15−D8, of which only bits D9 and D8 have meaning, and bits D15−D14 must be 01), followed by the least significant byte (bits D7−D0). The first two bytes are for the OTP register of the DAC addressed in step 3 above. This OTP register is automatically updated after receiving the second byte. The next two bytes are for the OTP register of the following DAC (bits D15−D14 must again be 01). That DAC OTP register is updated after receiving the fourth byte. This process continues until the registers of all following DAC OTP registers have been updated. The last address, 10100, is the address of the write disable bit and cannot be accessed using this method. It must be written using the write to a single OTP register procedure.
5. Send a STOP condition on the bus.

The BUF20820 will acknowledge each byte. To terminate communication, send a STOP or START condition on the bus. Only DAC registers that have received both bytes of data will be programmed.

OTP WRITE DISABLE

Writing a ‘1’ in bit D0 of register 10100 disables all future writes. The state of this bit can be accessed the same as any other data bit. It is important to set this bit to 1 after the OTP registers have been programmed to prevent accidental changes to the OTP registers. Until bit D0 of register 10100 is set to 1, any OTP register bit can be changed from 0 to 1; however, once a bit is set to a 1, it cannot be set back to 0.
SCL
Start Device Address Write Ackn DAC address pointer. D7−D5 must be 100. Ackn Stop
Write OperationGeneral acquire command. P4−P0 must specify any valid DAC address.
SDA_in A6 A5 A4 A3 A2 A1 A0 W Ackn D7 D6 D5 P4 P3 P2 P1 P0 Ackn
Device_out

SCL
Start Device Address Write Ackn DAC address pointer. D7−D5 must be 010. Ackn Stop
Write OperationSingle channel acquire command. P4−P0 must specify any valid DAC address.
SDA_in A6 A5 A4 A3 A2 A1 A0 W Ackn D7 D6 D5 P4 P3 P2 P1 P0 Ackn
Device_out

a) General Acquire

b) Single-Channel Acquire

Figure 9. Timing Diagram for Acquire Operation
a. Write Single DAC

Write single DAC register. P4−P0 specify DAC address.

If D15 = 0, the DACs are updated on the Latch pin.

If D15 = 1, all DACs are updated when the current DAC register is updated.

The whole DAC register D9−D0 is updated in this moment.

Device Address Write Ackn DAC address pointer. D7−D5 must be 000. Ackn DAC MSbyte. D14 must be 0. Ackn DAC LSbyte Ackn Stop

Device_out

Figure 10. Timing Diagram for Write DAC Register

b. Write Multiple DACs

Write multiple DAC registers. P4−P0 specify start DAC address.

If D15 = 0, the DACs are updated on the Latch pin.

If D15 = 1, all the DACs are updated when the current DAC register is updated.

The whole DAC register D9−D0 is updated in this moment.

Device_out

Figure 10. Timing Diagram for Write DAC Register
a. Read Single DAC

Start Device Address Write Ackn
DAC address pointer. D7−D5 must be 000. Ackn
Device Address Read Ackn DAC (pointer) MSbyte. D15−D10 have no meaning. Ackn
DAC LSbyte. No Ackn Stop

b. Read Multiple DACs

Figure 11. Timing Diagram for Read DAC Register
a) Write Single OTP Register

Device Address
Write Ackn
DAC address pointer. D7−D5 must be 000. Ackn DAC (pointer) MS Byte. D15−D14 must be 01. Ackn DAC (pointer) LS byte.

Start
Write Operation
SDA_in
W
Ackn
D7
D0
D5
P4−P0
Ackn
D15
D14
D13
D12
D11
D10
D9
D8
Ackn
D7
D6
D5
D4
D3
D2

The OTP register D9−D0 is updated at this moment.

t1 : >20
µs before falling edge of clock.

t2 : minimum 100
µs, maximum 2ms.

Figure 12. Timing Diagram for Write OTP Register

b) Write Multiple OTP Registers

Device Address
Write Ackn
Start DAC address pointer. D7−D5 must be 000. Ackn DAC (pointer) MS byte. D15−D14 must be 01. Ackn DAC (pointer + 1) MS byte.

Start
Write Operation
SDA_in
W
Ackn
D7
D0
D5
P4−P0
Ackn
D15
D14
D13
D12
D11
D10
D9
D8
Ackn
D7
D6
D5
D4
D3
D2
D1
D0

The whole DAC register D9−D0 is updated at this moment.

t1 : >20
µs before falling edge of clock.

t2 : minimum 100
µs, maximum 2ms.

Figure 12. Timing Diagram for Write OTP Register
REPLACEMENT OF TRADITIONAL GAMMA BUFFER

Traditional gamma buffers rely on a resistor string (often using expensive 0.1% resistors) to set the gamma voltages. During development, the optimization of these gamma voltages can be time consuming. Programming these gamma voltages with the BUF20820 can significantly reduce the time required for gamma voltage optimization. The final gamma values can be written into the internal OTP memory to replace a traditional gamma buffer solution. Figure 13a shows the traditional resistor string approach; Figure 13b shows the more efficient alternative method using the BUF20820.

The BUF20820 uses the most advanced high-voltage CMOS process available today, which allows it to be competitive with traditional gamma buffers. Programmability offers the following advantages:

- It shortens development time significantly.
- It eliminates manufacturing variance between panels.
- It allows a single panel to be built for multiple customers, with loading of customer-dependent gamma curves during final production. This significantly lowers inventory cost and risk and simplifies inventory management.
- It allows demonstration of various gamma curves to LCD monitor makers by simply uploading a different set of gamma values.
- It provides a simple means of adjusting gamma curves during final production improve picture quality and accommodate changes in the panel manufacturing process or end-customer requirements.
- It decreases cost and space.

Figure 13. Replacement of the Traditional Gamma Buffer
PROGRAMMABLE $V_{\text{COM}}$

The $V_{\text{COM}}$ channels of the BUF20820 can swing to 2.5V from the positive supply rail while sourcing 100mA, and to 1V above the negative rail while sinking 100mA (see Figure 4, typical characteristic Output Voltage vs Output Current). The gamma and the $V_{\text{COM}}$ values can be permanently stored in the internal OTP memory. The $V_{\text{COM}}$ channels can be programmed independently from the gamma channels. Figure 14 shows the BUF20820 being used for $V_{\text{COM}}$ voltages.

REFH AND REFL INPUT RANGE

Best performance and output swing range of the BUF20820 are achieved by applying REFH and REFL voltages that are slightly below the power-supply voltages. Most specifications have been tested at REFH = $V_S - 200\text{mV}$ and REFL = GND + 200mV. The REFH internal buffer is designed to swing very closely to $V_S$ and the REFL internal buffer to GND. However, there is a finite limit on how close they can swing before saturating. To avoid saturation of the internal REFH and REFL buffers, the REFH voltage should not be greater than $V_S - 100\text{mV}$ and REFL voltage should not be lower than GND + 100mV. Figure 15 shows the swing capability of the REFH and REFL buffers.

The other consideration when trying to maximize the output swing capability of the gamma buffers is the limitation in the swing range of output buffers (OUT1−18, $V_{\text{COM}}$ OUT1, and $V_{\text{COM}}$ OUT2), which depends on the load current. A typical load in the LCD application is 5−10mA. For example, if OUT1 is sourcing 10mA, the swing is typically limited to about $V_S - 200\text{mV}$. The same applies to OUT18, which typically limits at GND + 200mV when sinking 10mA. An increase in output swing can only be achieved for much lighter loads. For example, a 3mA load typically allows the swing to be increased to approximately $V_S - 100\text{mV}$ and GND + 100mV.

Connecting REFH directly to $V_S$ and REFL directly to GND does not damage the BUF20820. As discussed above however, the output stages of the REFH and REFL buffers will saturate. This condition is not desirable and can result in a small error in the measured output voltages of OUT1−18, $V_{\text{COM}}$ OUT1, and $V_{\text{COM}}$ OUT2. As described above, this method of connecting REFH and REFL does not help to maximize the output swing capability.

CONFIGURATION FOR 20 GAMMA CHANNELS

The $V_{\text{COM}}$ outputs can be used as additional gamma references in order to achieve two additional gamma channels (20 total). The $V_{\text{COM}}$ outputs will behave the same as the OUT1–9 outputs when sourcing or sinking smaller currents (see the Typical Characteristics, Figure 4). The $V_{\text{COM}}$ outputs are better able to swing to the positive rail than to the negative rail. Therefore, it is better to use the $V_{\text{COM}}$ outputs for higher reference voltages; see Figure 16.
CONFIGURATION FOR 22 GAMMA CHANNELS

In addition to the $V_{COM}$ outputs, the REFH and REFL OUT outputs can also be used as fixed gamma references. The output voltage will be set by the REFH and REFL input voltages, respectively. Therefore, REFH OUT should be used for the highest voltage gamma reference, and REFL OUT for the lowest voltage gamma reference. A 22-channel solution can be created by using all 18 outputs, the two $V_{COM}$ outputs, and both REFH/L OUT outputs for gamma references—see Figure 17. However, the REFH and REFL OUT buffers were designed to only drive light loads on the order of 5–10mA. Driving capacitive loads is not recommended with these buffers. In addition, the REFH and REFL buffers must not be allowed to saturate from sourcing/sinking too much current from REFH OUT or REFL OUT. Saturation of the REFH and REFL buffers results in errors in the voltages of OUT1–18, $V_{COM1}$, and $V_{COM2}$. The BUF01900 can be used to provide a programmable $V_{COM}$ output.

![Figure 16. 20-Gamma Channel Solution—2 $V_{COM}$ Channels Used as Additional Gamma Channels](image-url)
Figure 17. 22-Gamma Channel Solution
DYNAMIC GAMMA CONTROL

Dynamic gamma control is a technique used to improve the picture quality in LCD TV applications. The brightness in each picture frame is analyzed and the gamma curves are adjusted on a frame-by-frame basis. The gamma curves are typically updated during the short vertical blanking period in the video signal. Figure 18 shows a block diagram using the BUF20820 for dynamic gamma control and V_{COM} output.

The BUF20820 is ideally suited for rapidly changing the gamma curves because of its unique topology:

- double register input structure to the DAC;
- fast serial interface;
- simultaneous updating of all DACs by software. See the Read/Write Operations to write to all registers and the Output Latch sections.

The double register input structure saves programming time by allowing updated DAC values to be pre-loaded into the first register bank. Storage of this data can occur while a picture is still being displayed. Because the data are only stored into the first register bank, the DAC output values remain unchanged—the display is unaffected. During the vertical sync period, the DAC outputs (and therefore, the gamma voltages) can be quickly updated either by using an additional control line connected to the LD pin, or through software—writing a ‘1’ in bit 15 of any DAC register. For the details on the operation of the double register input structure, see the Output Latch section.

**Example:** Update all 18 gamma registers simultaneously via software.

**Step 1:** Check if LD pin is placed in HIGH state.

**Step 2:** Write DAC Registers 1–18 with bit 15 always ‘0’.

**Step 3:** Write any DAC register a second time with identical data. Make sure that bit 15 is ‘1’. All DAC channels will be updated simultaneously after receiving the last bit of data. (Note: this step may be eliminated by setting bit 15 of DAC 18 to ‘1’ in the previous step.)

---

![Diagram](image-url)  
**Figure 18. Dynamic Gamma Control**
TOTAL TI PANEL SOLUTION

In addition to the BUF20820 programmable voltage reference, TI offers a complete set of ICs for the LCD panel market, including gamma correction buffers, various power-supply solutions, and audio power solutions. See Figure 19 for the total IC solution from TI.

THE BUF20820 IN INDUSTRIAL APPLICATIONS

The wide supply range, high output current, and very low cost make the BUF20820 attractive for a range of medium accuracy industrial applications such as programmable power supplies, multi-channel data acquisition systems, data loggers, sensor excitation and linearization, power-supply generation, and others. Each DAC channel features 1LSB DNL and INL.

Many systems require different levels of biasing and power supply for various components as well as sensor excitation, control-loop set-points, voltage outputs, current outputs, and other functions. The BUF20820, with its 20 total programmable DAC channels, provides great flexibility to the entire system by allowing the designer to change all these parameters via software.

Figure 20 provides various ideas on how the BUF20820 can be used in applications. A micro-controller with two-wire serial interface controls the various DACs of the BUF20820. The BUF20820 can be used for:

- sensor excitation
- programmable bias/reference voltages
- variable power-supplies
- high-current voltage output
- 4-20mA output
- set-point generators for control loops.

NOTE: At power-up, the output voltages of the BUF20820 DACs are configured to the programmed OTP memory values, or \((V_{REFH} - V_{REFL})/2\) if the OTP values have not been programmed.

---

Figure 19. TI LCD Solution
Figure 20. Industrial Applications for the BUF20820
EVALUATION BOARD AND SOFTWARE

An evaluation board is available for the BUF20820, as shown in Figure 21. The evaluation board features easy-to-use software that allows individual channel voltages to be set. Configurations can be quickly evaluated to determine optimal codes for a given application. Contact your local TI representative for more information regarding the evaluation board.

Figure 21. BUF208x0 Evaluation Board
OUTPUT PROTECTION

The BUF20820 output stages can safely source and sink the current levels indicated in Figure 4. However, precautions must be taken in certain situations in order to prevent the output stages from being damaged by excessive current flow. The outputs (OUT1-18, V_{COM,OUT1} and V_{COM,OUT2}) include ESD protection diodes, as shown in Figure 22. Normally, these diodes do not conduct and are passive during typical device operation. Under certain operating conditions where the diodes may conduct, they can be subjected to high or even damaging current levels. These conditions are most likely to occur when a voltage applied to an output exceeds V_S + 0.5V, or drops below GND − 0.5V.

One common scenario where these conditions can occur is when the output pin is connected to a sufficiently large capacitor, and the BUF20820 power-supply source (V_S) is suddenly removed. Removing the power-supply source allows the capacitor to discharge through the current-steering diodes. The energy released during the high current flow period causes the power dissipation limits of the diode to be exceeded. Protection against this high current flow may be provided by placing current-limiting resistors in series with the output, as shown in Figure 8. Select a resistor value that restricts the current level to the maximum rating for the particular pin.

![Figure 22. Output Pins ESD Protection Current-Steering Diodes](image-url)
GENERAL POWERPAD DESIGN CONSIDERATIONS

The BUF20820 is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted, as shown in Figure 23(a) and Figure 23(b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see Figure 23(c). This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation. This provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the most negative supply voltage on the device, GND_A and GND_B.

1. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
2. Place recommended holes in the area of the thermal pad. Ideal thermal land size and thermal via patterns (2x5) for the HTSSOP-38 DCP package can be seen in the technical brief, PowerPAD Thermally-Enhanced Package (SLMA002), available for download at www.ti.com. These holes should be 13 mils (0.33mm) in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow.

3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the BUF20820 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.

4. Connect all holes to the internal plane that is at the same voltage potential as the GND pins.

5. When connecting these holes to the internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUF20820 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.

6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its eight holes exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.

7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

8. With these preparatory steps in place, the BUF20820 IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.
The thermal pad is electrically isolated from all terminals in the package.

**Figure 23. Views of Thermally-Enhanced DCP Package**

For a given $\theta_{JA}$, the maximum power dissipation is shown in Figure 24, and is calculated by Equation 3:

$$P_D = \left( \frac{T_{\text{MAX}} - T_A}{\theta_{JA}} \right)$$  \hspace{1cm} (3)

Where:

$P_D$ = maximum power dissipation (W)

$T_{\text{MAX}}$ = absolute maximum junction temperature (125°C)

$T_A$ = free-ambient air temperature (°C)

$\theta_{JA}$ = $\theta_{JC} + \theta_{CA}$

$\theta_{JC}$ = thermal coefficient from junction-to-case (°C/W)

$\theta_{CA}$ = thermal coefficient from case-to-ambient air (°C/W)

**Figure 24. Maximum Power Dissipation vs Free-Air Temperature (with PowerPAD soldered down)**
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>BUF20820AIDCPR</td>
<td>OBSOLETE</td>
<td>HTSSOP</td>
<td>DCP</td>
<td>38</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 85</td>
<td>BUF20820</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DCP (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

30 PIN SHOWN

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions, mold flash not to exceed 0.15mm.
⚠️ This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout.
This document is available at www.ti.com. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO-153

Table:

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