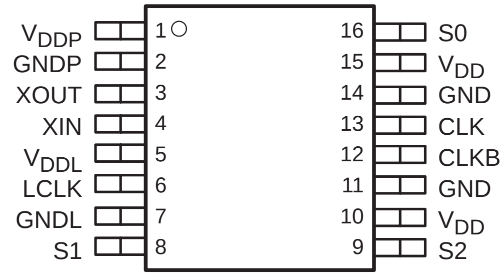
- **400-MHz Differential Clock Source for Direct Rambus Memory Systems for an 800-MHz Data Transfer Rate**
- **Operates From Two (3.3-V and 1.80-V) Power Supplies With 180 mW (Typ) at 400 MHz Total**
- **Packaged in a Thin Shrink Small-Outline Package (PW)**
- **External Crystal Required for Input**

PW PACKAGE
(TOP VIEW)

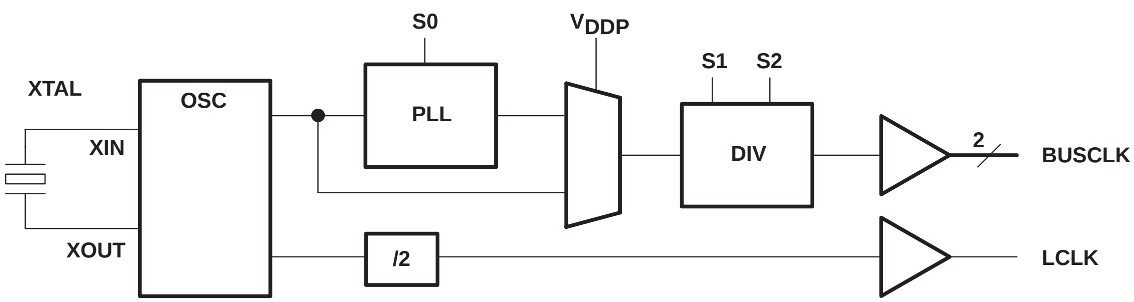


description

The Direct Rambus clock generator – lite (DRCG-Lite) is an independent crystal clock generator. It performs clock multiplication using PLL, sourced by an internal crystal oscillator. It provides one differential, high-speed Rambus channel compatible output pair. Also, one single-ended output is available to deliver 1/2 of the crystal frequency. The Rambus channel operates at up to 400 MHz with an option to select 300 MHz as well. The desired crystal is a 18.75-MHz crystal in a series resonance fundamental application.

The CDCR61A is characterized for operation over free-air temperatures of 0°C to 85°C.

functional block diagram



BUSCLK FREQUENCY SETTINGS

S0	M (PLL MULTIPLIER)
0	16
1 or Open	64/3

FUNCTION TABLE

V_{DDP}	S1	S2	MODE	CLK	CLKB	LCLK
ON	0	0	Normal	CLK	CLKB	XIN divided by 2
ON	1	1	Normal	CLK	CLKB	XIN divided by 2
ON	0	1	Test	Divided by 2	Divided by 2	XIN divided by 2
ON	1	0	Test	Divided by 4	Divided by 4	XIN divided by 2
0 V	0	0	Test	XIN	XIN (invert)	XIN divided by 2
0 V	1	1	Test	XIN	XIN (invert)	XIN divided by 2
0 V	0	1	Test	XIN divided by 2	XIN (invert) divided by 2	XIN divided by 2
0 V	1	0	Test	XIN divided by 4	XIN (invert) divided by 4	XIN divided by 2

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	13	O	Output clock, connect to Rambus channel
CLKB	12	O	Output clock (complement), connect to Rambus channel
GNDP, GNDL, GND	2, 7, 11, 14		Ground
LCLK	6	O	LVCMOS output, 1/2 of crystal frequency
S0, S1, S2	16, 8, 9	I	LVTTL level logic select terminal for function selection
V_{DD}	10, 15		Power supply, 3.3 V
V_{DDP}	1		Power supply for PLL, 3.3 V (0 V for Test mode)
V_{DDL}	5		Power supply for LCLK, 1.8 V
XIN	4	I	Reference crystal input
XOUT	3	O	Reference crystal feedback

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} or V_{DDP} (see Note 1) . . . . . –0.5 V to 4 V
Supply voltage range, V_{DDL} (see Note 1) . . . . . –0.5 V to 4 V
Input voltage range,V_I, at any input terminal . . . . . –0.5 V to V_{DD} + 0.5 V
Output voltage range, V_O, at any output terminal (CLK, CLKB) . . . . . –0.5 V to V_{DD} + 0.5 V
Output voltage range, V_O, at any output terminal (LCLK) . . . . . –0.5 V to V_{DDL} + 0.5 V
ESD rating (MIL-STD 883C, Method 3015) . . . . . > 2 kV, Machine Model >200 V
Continuous total power dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C‡	T_A = 85°C POWER RATING
PW	1400 mW	11 mW/°C	740 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		3	3.3	3.6	V
LCLK supply voltage, V_{DDL}		1.7	1.8	2.1	V
Low-level input voltage, V_{IL}	S0			0.35×V_{DD}	V
	S1, S2			0.35×V_{DD}	
High-level input voltage, V_{IH}	S0	0.65×V_{DD}			V
	S1, S2	0.65×V_{DD}			
Internal pullup resistance	S0	10	55	100	kΩ
	S1, S2	90	145	250	
Low-level output current, I_{OL}	CLK, CLKB			16	mA
	LCLK			10	
High-level output current, I_{OH}	CLK, CLKB			–16	mA
	LCLK			–10	
Input frequency at crystal input		14.0625	18.75		MHz
Input capacitance (CMOS), C_I†	S0, S1, S2			2.5	pF
	XIN, XOUT			20	
Operating free-air temperature, T_A		0		85	°C

† Capacitance measured at f = 1 MHz, dc bias = 0.9 V, and V_{AC} < 100 mV

timing requirements

	MIN	MAX	UNIT
Clock cycle time, $t_{(cycle)}$	2.5	3.7	ns
Input slew rate, SR	0.5	4	V/ns
State transition latency (V_{DDX} or S0 to CLKs – normal mode), $t_{(STL)}$		3	ms

crystal specifications

	MIN	MAX	UNIT
Frequency	14.0625	18.75	MHz
Frequency tolerance (at 25°C ±3°C)	–15	15	ppm
Equivalent resistance (C_L = 10 pF)		100	Ω
Temperature drift (–10°C to 75°C)		10	ppm
Drive level	0.01	1500	µW
Motional inductance	20.7	25.3	mH
Insulation resistance	500		MΩ
Spurious attenuation ratio (at frequency ±500 kHz)	3		dB
Overtone spurious	8		dB

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{O(X)}$	Differential crossing-point output voltage		See Figures 1 and 7		1.25		1.85	V
$V_{O(PP)}$	Peak-to-peak output voltage swing, single ended		$V_{OH} – V_{OL}$,	See Figure 1	0.4		0.7	V
V_{IK}	Input clamp voltage		V_{DD} = 3 V,	I_I = –18 mA			–1.2	V
R_I	Input resistance	XIN, XOUT	V_{DD} = 3.3 V,	$V_I = V_O$		>50		kΩ
I_{IH}	High-level input current	XOUT	V_{DD} = 3.3 V,	V_O = 2 V			27	mA
		S0	V_{DD} = 3.6 V,	$V_I = V_{DD}$			10	μA
		S1, S2	V_{DD} = 3.6 V,	$V_I = V_{DD}$			10	
I_{IL}	Low-level input current	XOUT	V_{DD} = 3.3 V,	V_O = 0 V			–5.7	mA
		S0	V_{DD} = 3.6 V,	V_I = 0 V	–30		–100	μA
		S1, S2	V_{DD} = 3.6 V,	V_I = 0 V	–10		–50	
V_{OH}	High-level output voltage	CLK, CLKB	See Figure 1				2.1	V
			V_{DD} = min to max,	I_{OH} = –1 mA	V_{DD}– 0.1 V			
			V_{DD} = 3 V,	I_{OH} = –16 mA	2.2			
		LCLK	V_{DDL} = min to max,	I_{OH} = – 10 mA	V_{DDL} – 0.45 V		V_{DDL}	
V_{OL}	Low-level output voltage	CLK, CLKB	See Figure 1		1			V
			V_{DD} = min to max,	I_{OL} = 1 mA			0.1	
			V_{DD} = 3 V,	I_{OL} = 16 mA			0.5	
		LCLK	V_{DDL} = min to max,	I_{OL} = 10 mA	0		0.45	
I_{OH}	High-level output current	CLK, CLKB	V_{DD} = 3.135 V,	V_O = 1 V	–32	–52		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V		–51		
			V_{DD} = 3.465 V,	V_O = 3.135 V		–14.5	–21	
		LCLK	V_{DDL} = 1.7 V,	V_O = 0.5 V	–11	–26		
			V_{DDL} = 1.8 V,	V_O = 0.9 V		–28		
			V_{DDL} = 2.1 V,	V_O = 1.6 V		–24.5	–35	
I_{OL}	Low-level output current	CLK, CLKB	V_{DD} = 3.135 V,	V_O = 1.95 V	43	61.5		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V		65		
			V_{DD} = 3.465 V,	V_O = 0.4 V		25.5	36	
		LCLK	V_{DDL} = 1.7 V,	V_O = 1.2 V	11	27		
			V_{DDL} = 1.8 V,	V_O = 0.9 V		30		
			V_{DDL} = 2.1 V,	V_O = 0.5 V		28	38	
r_{OH}	High-level dynamic output resistance§		ΔI_O – 14.5 mA to ΔI_O – 16.5 mA		12	25	40	Ω
r_{OL}	Low-level dynamic output resistance§		ΔI_O + 14.5 mA to ΔI_O + 16.5 mA		12	17	40	Ω
C_O	Output capacitance	CLK, CLKB					3	pF
		LCLK					3	

† V_{DD} refers to any of the following; V_{DD}, V_{DDL}, and V_{DDP}
‡ All typical values are at V_{DD} = 3.3 V, V_{DDL} = 1.8 V, T_A = 25°C.
§ $r_O = \Delta V_O / \Delta I_O$. This is defined at the output terminals, not at the measurement point of Figure 1.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
I_{DD}	Static supply current	Outputs high or low (V_{DDP} = 0 V)			6.5	mA
I_{DDL}	Static supply current (LVCMOS)	Outputs high or low (V_{DDP} = 0 V)			50	µA
$I_{DD(NORMAL)}$	Supply current in normal state	300 MHz			39	mA
		400 MHz			50	mA
$I_{DDL(NORMAL)}$	Supply current in normal state (LVCMOS)	400 MHz			8	mA

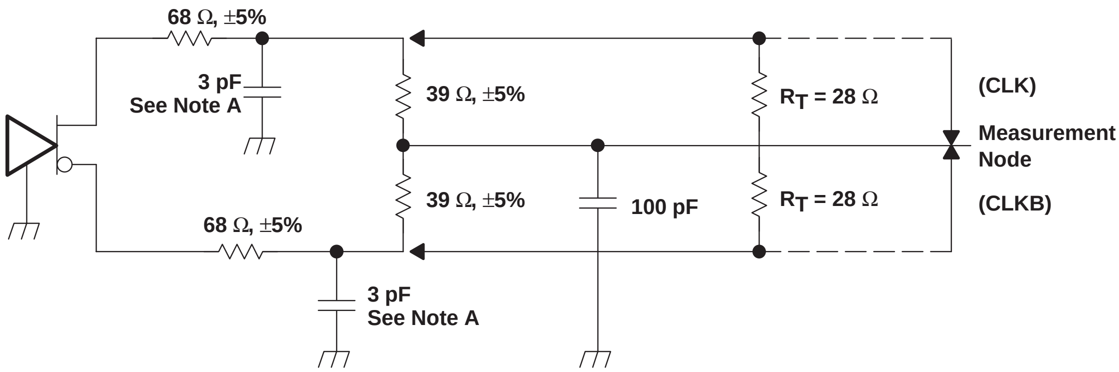
† V_{DD} refers to any of the following; V_{DD}, V_{DDL}, and V_{DDP}
‡ All typical values are at V_{DD} = 3.3 V, V_{DDL} = 1.8 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{(cycle)}$	Clock cycle time (CLK, CLKB)			2.5		3.7	ns
t_{cj}	Total jitter over 1, 2, 3, 4, 5, or 6 clock cycles‡	300 MHz	See Figure 3			140	ps
		400 MHz				100	
t_{jL}	Long-term jitter	300 MHz	See Figure 4			400	ps
		400 MHz				300	
t_{DC}	Output duty cycle over 10,000 cycles		See Figure 5	45%		55%	
$t_{DC,ERR}$	Output cycle-to-cycle duty cycle error	300 MHz	See Figure 6			70	ps
		400 MHz				55	
t_r, t_f	Output rise and fall times (measured at 20%-80% of output voltage)#	CLK, CLKB	See Figure 9,	160		400	ps
Δt	Difference between rise and fall times on a single device (20%–80%) $\lvert t_f - t_r \rvert$#		See Figure 9,			100	ps
$t_{c(LCLK)}$	Clock cycle time (LCLK)			106.6		142.2	ns
$t_{(cj)}$	LCLK cycle jitter§		See Figure 11	–0.2		0.2	ns
$t_{(cj10)}$	LCLK 10-cycle jitter§¶		See Figure 11	–1.3 $t_{(cj)}$		1.3 $t_{(cj)}$	ns
t_{DC}	Output duty cycle	LCLK		40%		60%	
t_r, t_f	Output rise and fall times (measured at 20%-80% of output voltage)	LCLK	See Figure 9			1	ns
	PLL loop bandwidth		f_{mod} = 50 kHz			–3	dB
			f_{mod} = 8 MHz	–20			

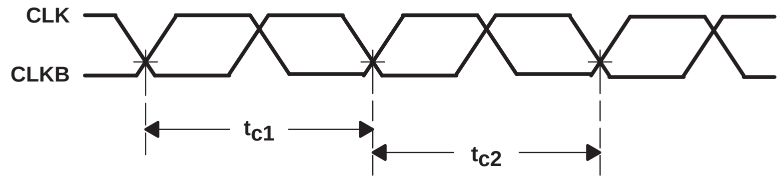
† All typical values are at V_{DD} = 3.3 V, T_A = 25°C.
‡ Output short-term jitter specification is peak-to-peak (see Figure 9).
§ LCLK cycle jitter and 10-cycle jitter are defined as the difference between the measured period and the nominal period.
¶ LCLK 10-cycle jitter specification is based on the measured value of LCLK cycle jitter.
# V_{DD}= 3.3 V

PARAMETER MEASUREMENT INFORMATION



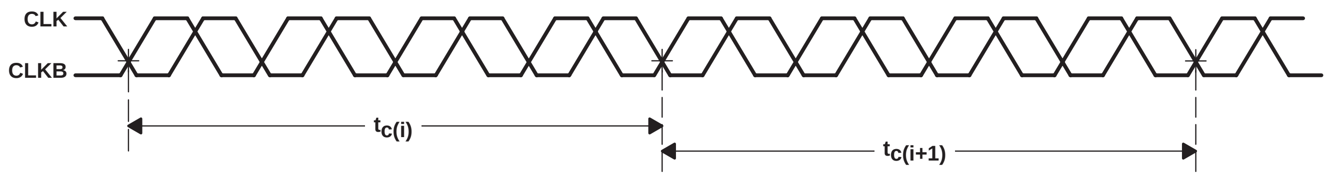
NOTE A: These capacitors represent parasitic capacitance. No discrete capacitors are used on the test board during device characterization.

Figure 1. Test Load and Voltage Definitions ($V_{O(STOP)}$, $V_{O(X)}$, V_O, V_{OH}, V_{OL})



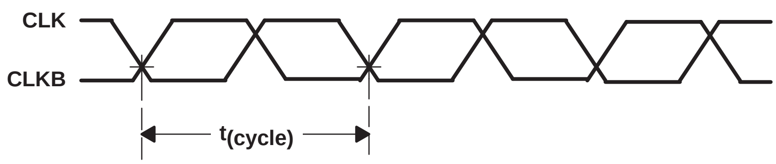
Cycle-to-cycle jitter = | $t_{c1} - t_{c2}$| over 10000 consecutive cycles

Figure 2. Cycle-to-Cycle Jitter



$t_{c(i)}$ = nominal expected time
Cycle-to-cycle jitter = | $t_{c(i)} - t_{c(i+1)}$| over 10000 consecutive cycles

Figure 3. Short-Term Cycle-to-Cycle Jitter over 2, 3, 4, or 6 Cycles



t_{jL} = | $t_{(cycle), max} - t_{(cycle), min}$| over 10000 consecutive cycles

Figure 4. Long-Term Jitter

PARAMETER MEASUREMENT INFORMATION

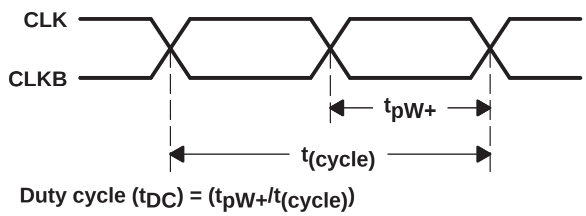


Figure 5. Output Duty Cycle

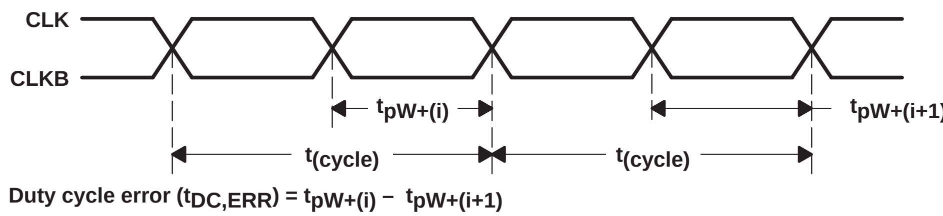


Figure 6. Duty Cycle Error (Cycle-to-Cycle)

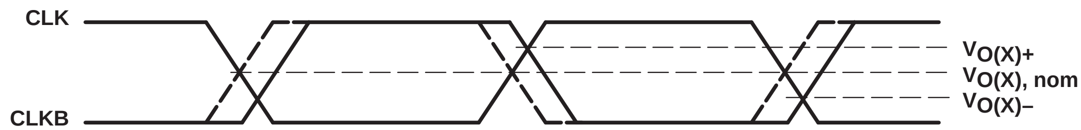


Figure 7. Crossing-Point Voltage

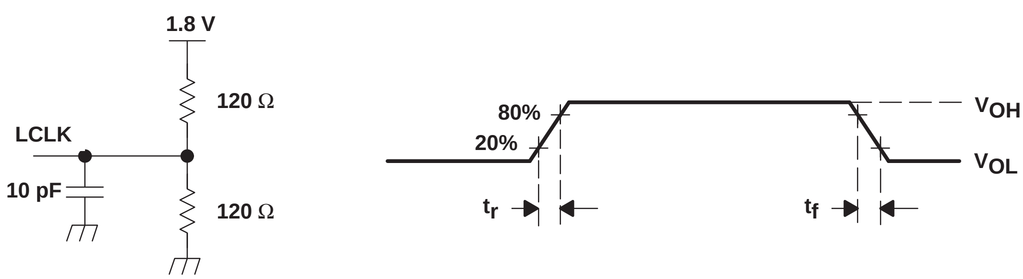


Figure 8. LCLK Test Load Circuit and Voltage Waveform for CLK/CLKB and LCLK

PARAMETER MEASUREMENT INFORMATION

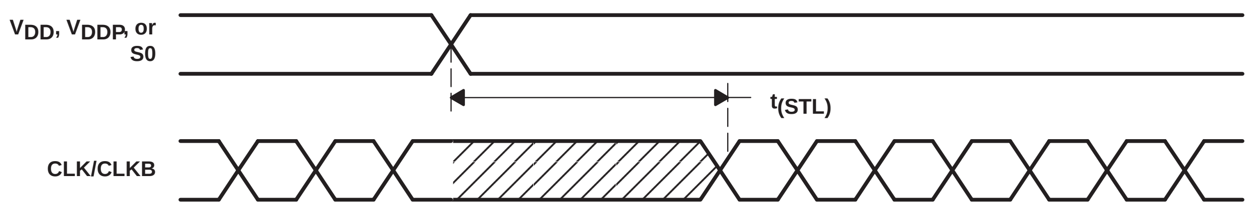


Figure 9. PLL Frequency Transition Timing

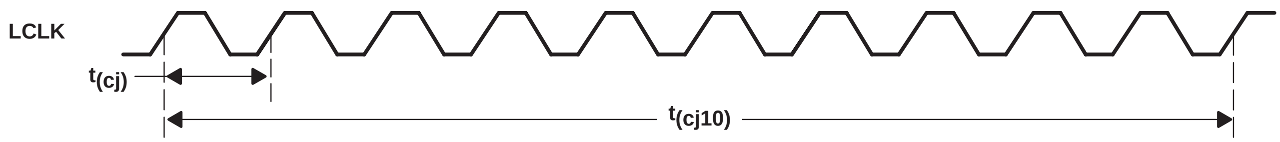


Figure 10. LCLK Jitter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCR61APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKR61A	Samples
CDCR61APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKR61A	Samples
CDCR61APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKR61A	Samples
CDCR61APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKR61A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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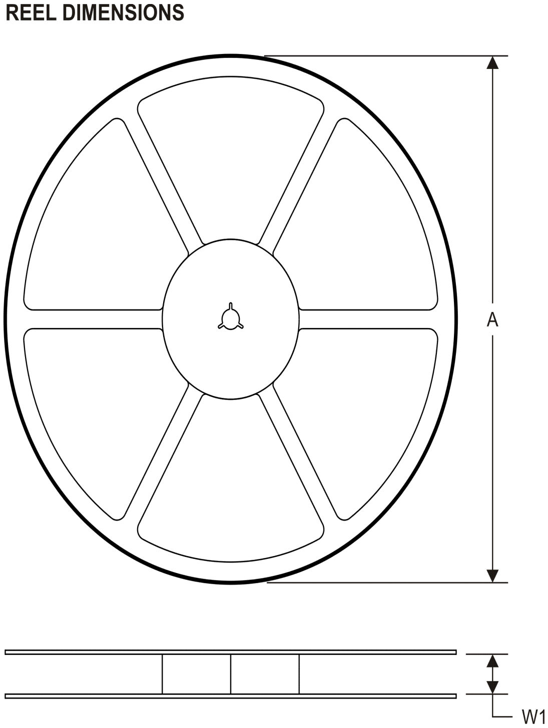
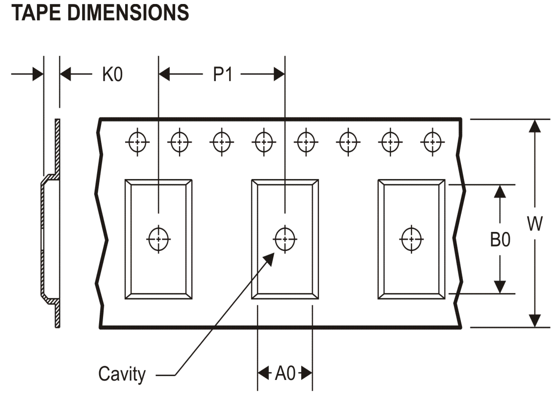
TAPE AND REEL INFORMATION





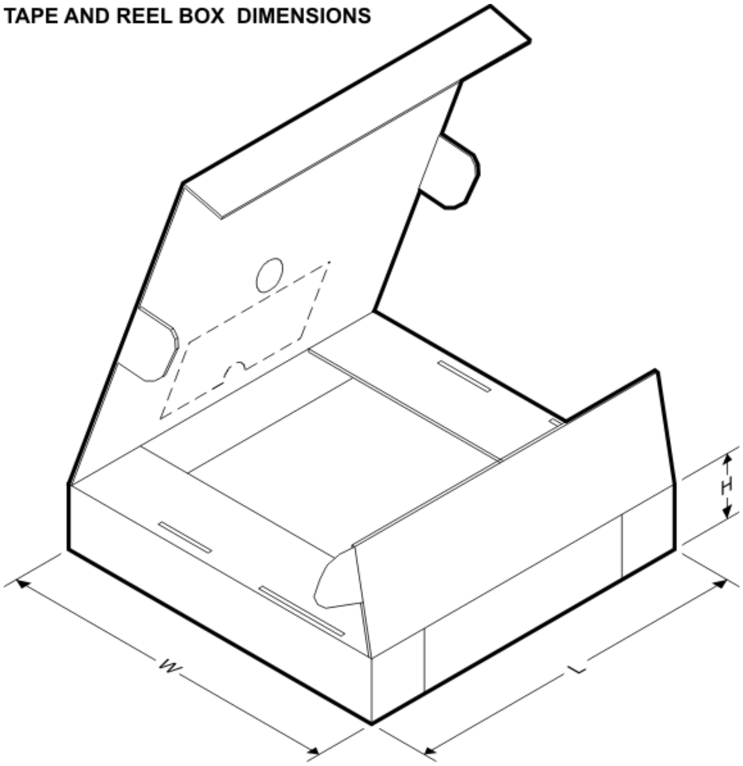
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCR61APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

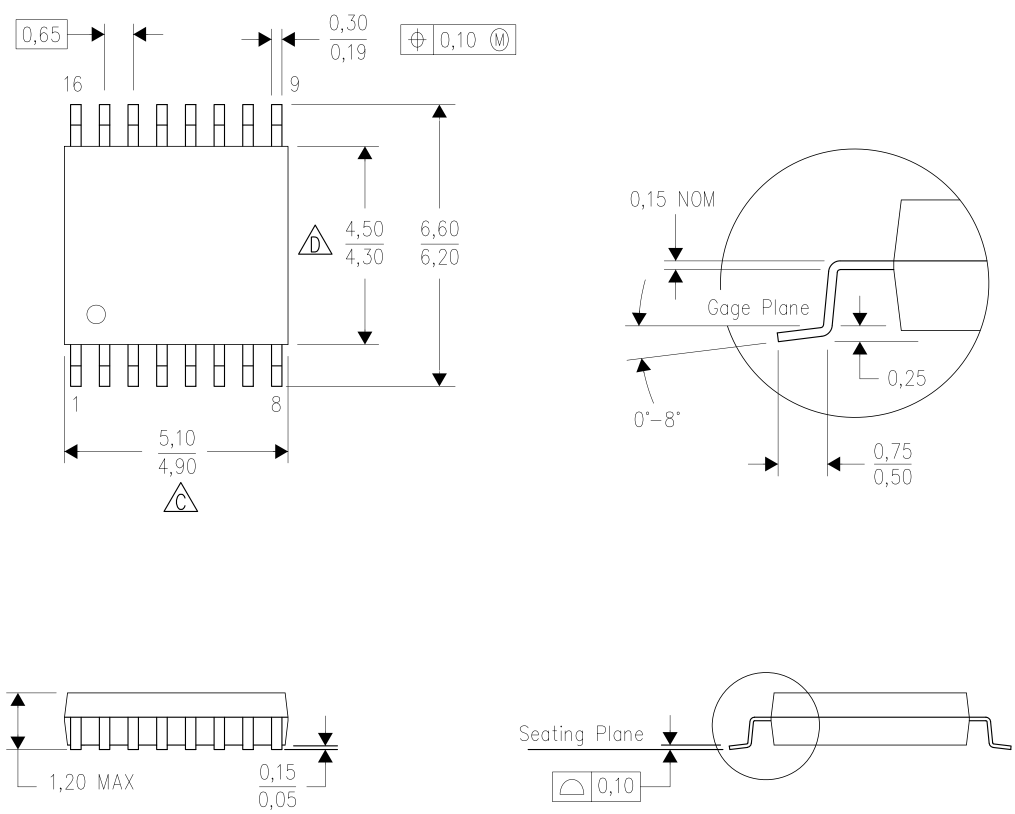
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCR61APWR	TSSOP	PW	16	2000	367.0	367.0	35.0

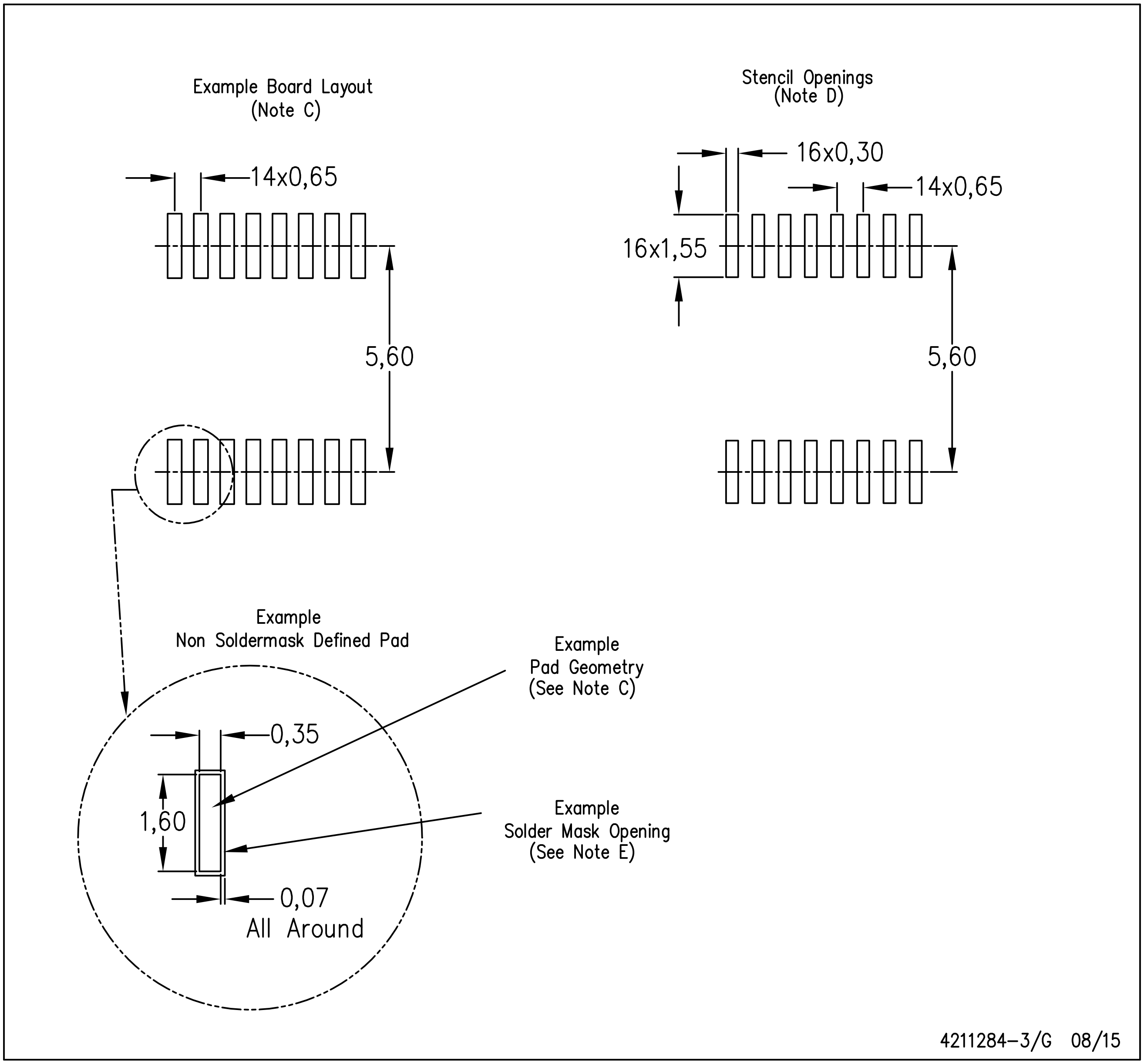
PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



4040064-4/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

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