

FM STEREO TRANSMITTER

Check for Samples: [SN761634](#)

FEATURES

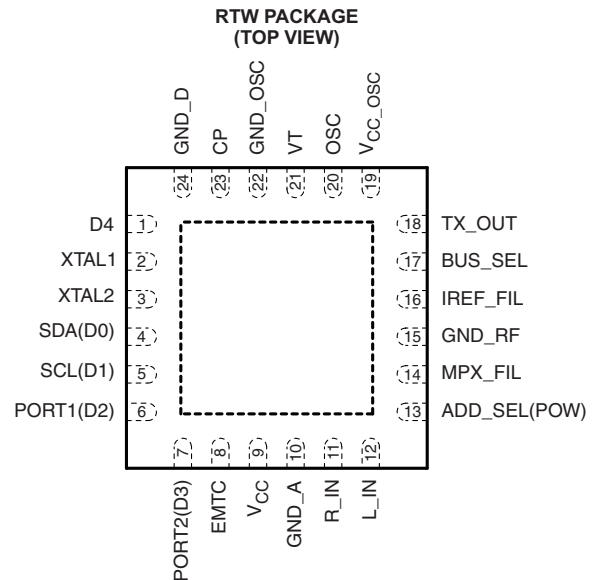
- Single-Chip FM Stereo Transmitter
- Selectable I²C/Parallel Control Mode
- V_{CC} = 2.5 V to 4 V
- 76-MHz to 108-MHz Transmit Frequency Range
- Selectable –7-, –3-, 1-, 4-dBm Tx High-Power Output
- I_{CC} = 12 mA (Depends on Tx Power)
- 32.768-kHz Clock
- 24-Pin Quad Flatpack No Lead (QFN) Package, 4 × 4 mm
- Standby
- Fourth Order 15-kHz Low Pass Filter (LPF)

APPLICATIONS

- Portable Audio Players
- MP3 Players
- Personal Navigation Devices (PNDs)
- Portable Media Players (PMPs)

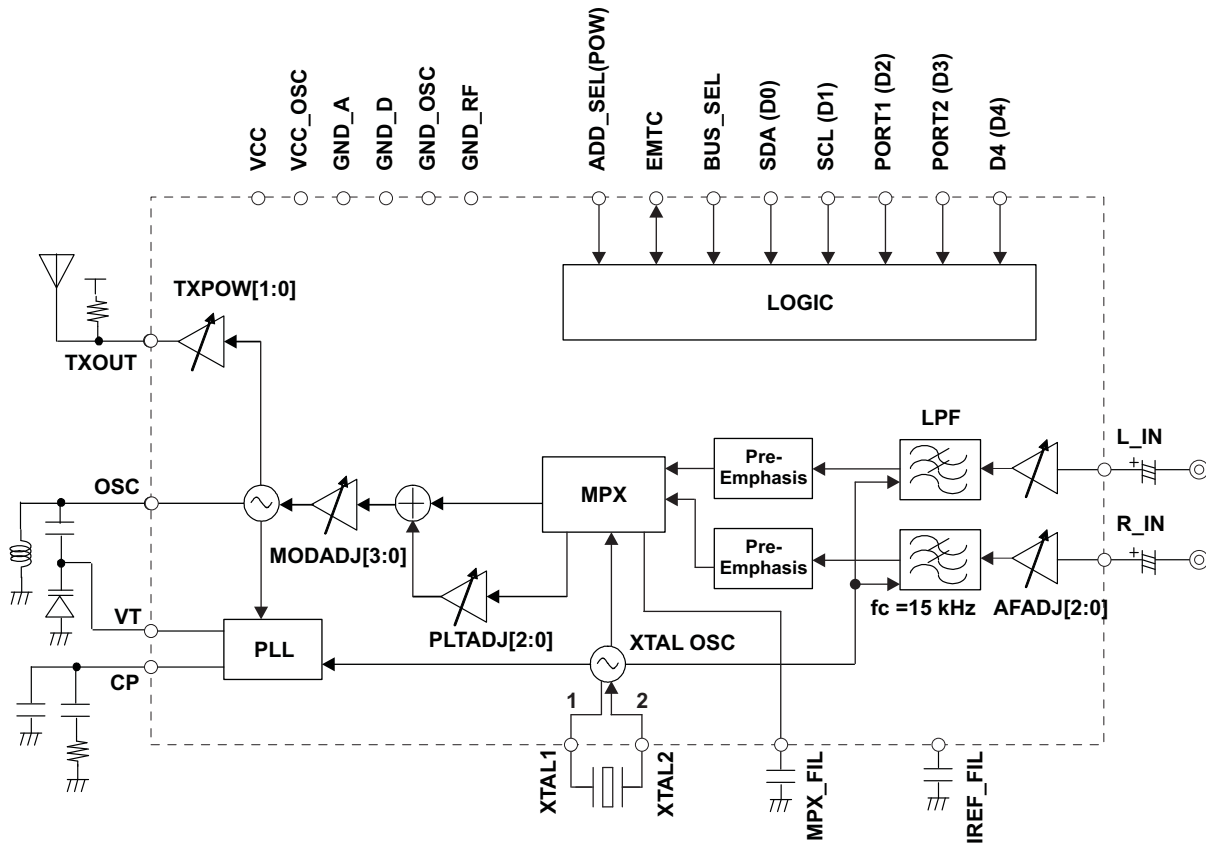
DESCRIPTION

The SN761634 is an FM stereo transmitter IC for portable audio players.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FM TRANSMITTER BLOCK



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION	SCHEMATIC
NO.	NAME		
1	D4(D4)	To be connected to ground in I ² C mode / D4 input in parallel mode	Figure 1
2	XTAL1	Crystal oscillator	Figure 2
3	XTAL2	Crystal oscillator	Figure 2
4	SDA(D0)	I ² C data input/output in I ² C mode/ D0 input in parallel mode	Figure 3
5	SCL(D1)	I ² C clock input / D1 input in parallel mode	Figure 4
6	PORT1(D2)	Port 1 output in I ² C mode / D2 input in parallel mode	Figure 5
7	PORT2(D3)	Port 2 output in I ² C mode / D3 input in parallel mode	Figure 5
8	EMTC	To be opened in I ² C mode / EMTC input in parallel mode	Figure 6
9	V _{CC}	Power supply	
10	GND_A	Analog ground	
11	R_IN	Audio right input	Figure 7
12	L_IN	Audio left input	Figure 7
13	ADD_SEL(POW)	I ² C address select in I ² C mode / TX power select in parallel mode	Figure 8
14	MPX_FIL	MPX PLL filter	Figure 9
15	GND_RF	RF ground	
16	IREF_FIL	Reference current filter	Figure 10
17	BUS_SEL	I ² C mode / Parallel mode select	Figure 11
18	TX_OUT	Transmitter output	Figure 12
19	V _{CC_osc}	Oscillator power supply	
20	OSC	Oscillator input	Figure 13
21	VT	Tuning voltage output	Figure 14
22	GND_OSC	Oscillator ground	
23	CP	Charge pump output	Figure 14
24	GND_D	Digital ground	

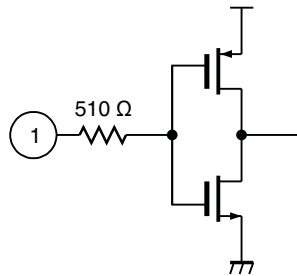


Figure 1. D4

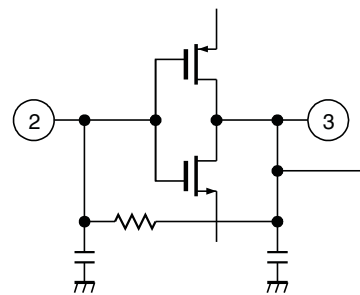


Figure 2. XTAL1 and XTAL2

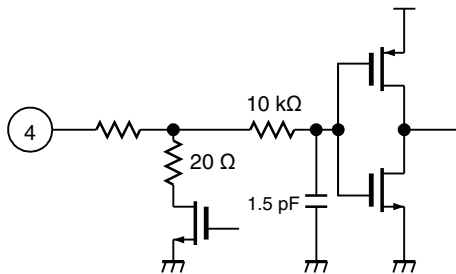


Figure 3. SDA(D0)

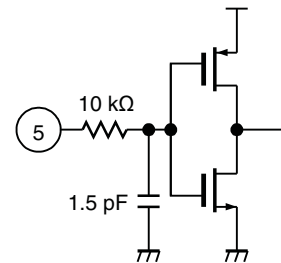


Figure 4. SCL(D1)

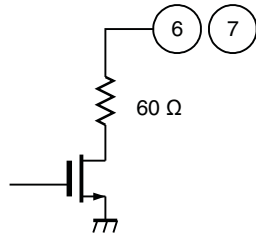


Figure 5. PORT1(D2) and PORT2(D3)

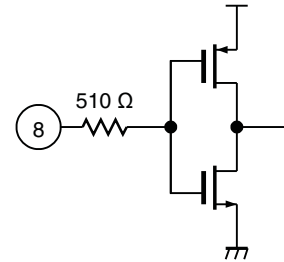


Figure 6. EMTC

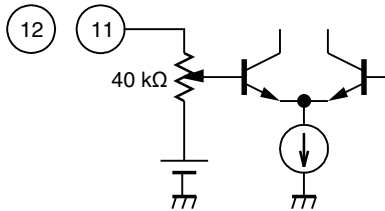


Figure 7. RIN and LIN

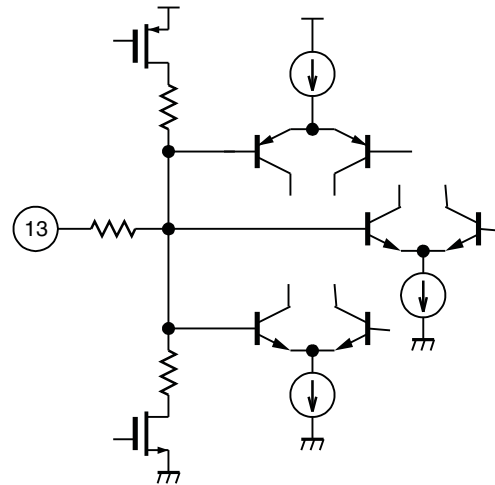


Figure 8. ADD_SEL(POW)

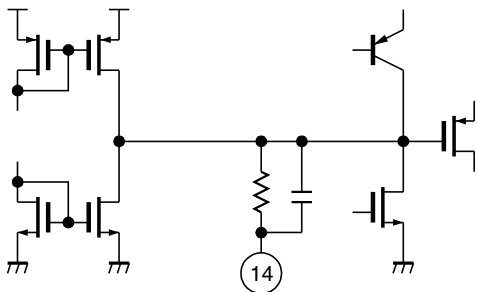


Figure 9. MPX FIL

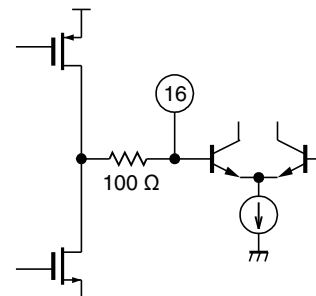


Figure 10. IREF FIL

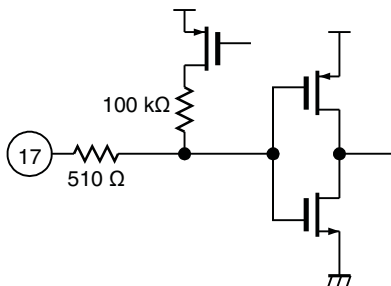


Figure 11. BUS_SEL

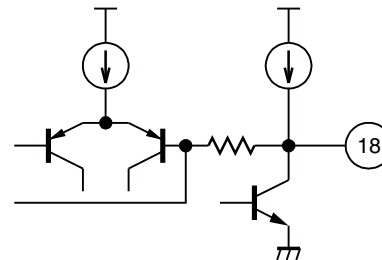


Figure 12. TX_OUT

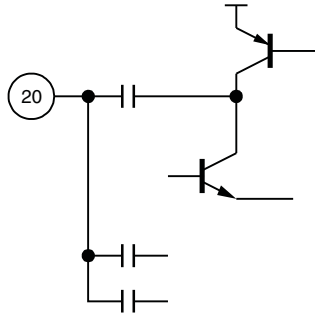


Figure 13. OSC

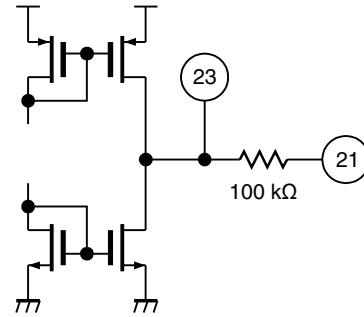


Figure 14. VT and CP

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	V_{CC}, V_{CC_osc}	-0.3	6.0	V
V_{IN}	Input voltage	Other pins	-0.3	V_{CC}	V
T_A	Operating free-air temperature range		-20	85	°C
T_{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	V_{CC}, V_{CC_osc}	2.5	3	4	V
T_A	Operating free-air temperature		-20		85	°C



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

$V_{CC} = 3\text{ V}$, $T_A = 25^\circ\text{C}$, RF frequency $f_{RF} = 98.1\text{ MHz}$, BAND = 0 (USEU), TXPOW[1:0] = -7 dBm, MODADJ[3:0] = 5 dB (for 98.1 MHz), audio signal frequency $f_{AF} = 1\text{ kHz}$, 100% means FM 75 kdev, BW = LPF 30 kHz, measured with typical home hi-fi tuner. (unless otherwise noted)

Supply Voltages and Currents

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	V_{CC} and V_{CC_OSC} are the same voltage			V
$I_{CC\ TX1}$	Tx mode supply current 1	No L_IN, R_IN input, TXPOW[1:0] = 00, $R_{TX} = \text{open}$			mA
$I_{CC\ TX2}$	Tx mode supply current 2	No L_IN, R_IN input, TXPOW[1:0] = 00, $R_{TX} = \text{open}$, DIS AFLPF = 1			mA
$I_{CC\ TX3}$	Tx mode supply current 3	No L_IN, R_IN input, TXPOW[1:0] = 10, $R_{TX} = 300\ \Omega$			mA
$I_{CC\ TX4}$	Tx mode supply current 4	No L_IN, R_IN input, TXPOW[1:0] = 11, $R_{TX} = 150\ \Omega$			mA
$I_{CC\ STBY1}$	Standby current 1	STBY bit = 1 in I ² C mode			μA
$I_{CC\ STBY2}$	Standby current 2	D4, D3, D2, D1, D0 = 0, 0, 0, 0 in parallel mode			μA

Crystal Oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{XTAL}	Crystal oscillator frequency	Crystal $C_L = 12.5\text{ pF}$			kHz

Voltage Controlled Oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency range	150		217	MHz

Synthesizer

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
N	Programmable counter	14 bit		271	16383
f_{REF}	Reference frequency for phase detector		8.192		kHz
f_{STEP}	Tuning frequency step		8.192		kHz
I_{CP}	Charge pump current	CP[1:0] = 00	0.6		μA
		CP[1:0] = 01	1.25		
		CP[1:0] = 10	2.5		
		CP[1:0] = 11	50		

RF Power

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TXOUT}	TX output power	TXPOW[1:0] = 00, $R_{TX} = \text{open}$, $R_L = 50\ \Omega$	-7		dBm
		TXPOW[1:0] = 01, $R_{TX} = 300\ \Omega$, $R_L = 50\ \Omega$	-3		
		TXPOW[1:0] = 10, $R_{TX} = 300\ \Omega$, $R_L = 50\ \Omega$	1		
		TXPOW[1:0] = 11, $R_{TX} = 150\ \Omega$, $R_L = 50\ \Omega$	4		

AF Power

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AF _{ADJ}	AF input level adjust ratio	AFADJ [2:0] = 000		-9		dB
		AFADJ [2:0] = 001		-6		
		AFADJ [2:0] = 010		-3		
		AFADJ [2:0] = 011 (Ref.)		0		
		AFADJ [2:0] = 100		3		
		AFADJ [2:0] = 101		6		
		AFADJ [2:0] = 110		9		
		AFADJ [2:0] = 111		12		
V _{IMAX50}	AF maximum input level (pre-emphasis 50 μs)	AFADJ = 0 dB, EMTC = 0, f _s = 400 Hz, L = R each channel			1000	mVpp
		AFADJ = 0 dB, EMTC = 0, f _s = 10 kHz, L = R each channel			330	mVpp
V _{IMAX75}	AF maximum input level (pre-emphasis 75 μs)	AFADJ = 0 dB, EMTC = 1, f _s = 400 Hz, L = R each channel			1000	mVpp
		AFADJ = 0 dB, EMTC = 1, f _s = 10 kHz, L = R each channel			200	mVpp
V _{IAF}	AF typical input level for 100% dev	AFADJ = 0 dB, f _s = 400 Hz, DIS_EM = 0, L = R each channel		250		mVrms
f _{IAFR}	Input frequency range		20		15 k	Hz
R _{IAF}	AF input impedance			40		kΩ
t _{PRE}	Pre-emphasis	EMTC bit = 0		50		μs
		EMTC bit = 1		75		
f _{LPF}	AFLPF frequency response	DIS_AFLPF = 0, -3 dB		15		kHz

Mono Mode

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{O MONO}	Output frequency response	CP = 1.25 μA	20		15 k	Hz
S/N _{MONO98}	Mono S/N at 98.1 MHz (100% modulation)	L = R = 250 mVrms, f _{AF} = 1 kHz, AFADJ = 0 dB, MODADJ = 5 dB, PLTADJ = off, MONO_ST = 1, RF = 98.1 MHz, BAND = 0		60		dB
THD _{MONO98}	Mono THD at 98.1 MHz (30% modulation)	L = R = 75 mVrms, f _{AF} = 1 kHz, AFADJ = 0 dB, MODADJ = 5 dB, PLTADJ = off, MONO_ST = 1, RF = 98.1 MHz, BAND = 0		0.5		%
S/N _{MONO83}	Mono S/N at 83 MHz (100% modulation)	L = R = 250 mVrms, f _{AF} = 1 kHz, AFADJ = 0 dB, MODADJ = 11 dB, PLTADJ = off, MONO_ST = 1, RF = 83.0 MHz, BAND = 1		60		dB
THD _{MONO83}	Mono THD at 83 MHz (30% modulation)	L = R = 75 mVrms, f _{AF} = 1 kHz, AFADJ = 0 dB, MODADJ = 11 dB, PLTADJ = off, MONO_ST = 1, RF = 83.0 MHz, BAND = 1		0.5		%
ATT _{MT MONO}	MUTE attenuation	MUTE bit = 1	50			dB

Stereo Mode

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
S/N _{ST98}	Stereo S/N at 98.1 MHz Main + sub = 90%, pilot = 10%	L = R = 225 mVrms, $f_{AF} = 1$ kHz, AFADJ = 0 dB, MODADJ = 5 dB, PLTADJ = 0 dB, $f_{RF} = 98.1$ MHz, BAND = 0		55		dB
SEP _{ST98}	Stereo separation at 98.1 MHz Main + sub = 30%, pilot = 10%	L or R = 75 mVrms, $f_{AF} = 1$ kHz, AFADJ = 0 dB, PLTADJ = 0 dB, MODADJ = 5 dB, $f_{RF} = 98.1$ MHz, BAND = 0		30		dB
THD _{ST98}	Stereo THD at 98.1 MHz Main + sub = 30%, pilot = 10%	L or R = 75 mVrms, $f_{AF} = 1$ kHz, AFADJ = 0 dB, PLTADJ = 0 dB, MODADJ = 5 dB, $f_{RF} = 98.1$ MHz, BAND = 0		1.0		%
S/N _{ST83}	Stereo S/N at 83.0 MHz Main + sub = 90%, pilot = 10%	L = R = 225 mVrms, $f_{AF} = 1$ kHz, AFADJ = 0 dB, PLTADJ = 0 dB, MODADJ = 11dB, $f_{RF} = 83.0$ MHz, BAND = 1		55		dB
SEP _{ST83}	Stereo separation at 83.0 MHz Main + sub = 30%, pilot = 10%	L or R = 75 mVrms, $f_{AF} = 1$ kHz, AFADJ = 0 dB, MODADJ = 11 dB, PLTADJ = 0 dB, $f_{RF} = 83.0$ MHz, BAND = 1		30		dB
THD _{ST83}	Stereo THD at 83.0 MHz Main + sub = 30%, pilot = 10%	L or R = 75 mVrms, $f_{AF} = 1$ kHz, AFADJ = 0 dB, MODADJ = 11 dB, PLTADJ = 0 dB, $f_{RF} = 83.0$ MHz, BAND = 1		1.0		%
DIFF _{ST MOD}	Left channel and right channel modulation difference	L = R = 75 mVrms, $f_{AF} = 1$ kHz, AFADJ = 0 dB, MODADJ = 11 dB, PLTADJ = 0 dB, $f_{RF} = 98.1$ MHz, BAND = 1 Lch level Ref.	-1		1	dB

Modulation

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOD _{RA} DJ	Modulation adjust ratio	MODADJ[3:0] = 0000 (Ref.)		0		dB
		MODADJ[3:0] = 0001		1		
		MODADJ[3:0] = 0010		2		
		MODADJ[3:0] = 0011		3		
		MODADJ[3:0] = 0100		4		
		MODADJ[3:0] = 0101		5		
		MODADJ[3:0] = 0110		6		
		MODADJ[3:0] = 0111		7		
		MODADJ[3:0] = 1000		8		
		MODADJ[3:0] = 1001		9		
		MODADJ[3:0] = 1010		10		
		MODADJ[3:0] = 1011		11		
		MODADJ[3:0] = 1100		12		
		MODADJ[3:0] = 1101		13		
		MODADJ[3:0] = 1110		14		
MODADJ[3:0] = 1111		15				
MOD _{MONO} 76	TX mono modulation at 76.0 MHz	L = R = 250 mVrms, $f_{AF} = 1$ kHz, AFADJ = 0 dB, PLTADJ = off, MONO_ST = 1, MODADJ = 13 dB, BAND = 1		75		kHzdev
MOD _{MONO} 83	TX mono modulation at 83.0 MHz	L = R = 250 mVrms, $f_{AF} = 1$ kHz, AFADJ = 0 dB, PLTADJ = off, MONO_ST = 1, MODADJ = 11 dB, BAND = 1		75		kHzdev
MOD _{MONO} 90	TX mono modulation at 90.0 MHz	L = R = 250 mVrms, $f_{AF} = 1$ kHz, AFADJ = 0 dB, PLTADJ = off, MONO_ST = 1, MODADJ = 8 dB, BAND = 1		75		kHzdev
MOD _{MONO} 87	TX mono modulation at 87.5 MHz	L = R = 250 mVrms, $f_{AF} = 1$ kHz, AFADJ = 0 dB, PLTADJ = off, MONO_ST = 1, MODADJ = 9 dB, BAND = 0		75		kHzdev

Modulation (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOD _{MONO98}	TX mono modulation at 98.1 MHz	L = R = 250 mVrms, f _{AF} = 1 kHz, AFADJ = 0 dB, PLTADJ = off, MONO_ST = 1, MODADJ = 5 dB, BAND = 0		75		kHzdev
MOD _{MONO108}	TX mono modulation at 108.0 MHz	L = R = 250 mVrms, f _{AF} = 1 kHz, AFADJ = 0 dB, PLTADJ = off, MONO_ST = 1, MODADJ = 3 dB, BAND = 0		75		kHzdev
MOD _{RPLT}	Pilot modulation adjust ratio	PLTADJ[2:0] = 000		-6		dB
		PLTADJ[2:0] = 001		-4		
		PLTADJ[2:0] = 010		-2		
		PLTADJ[2:0] = 011 (Ref.)		0		
		PLTADJ[2:0] = 100		2		
		PLTADJ[2:0] = 101		4		
		PLTADJ[2:0] = 110		6		
MPLT _{TYP}	Typical pilot modulation	L = R = 225 mVrms, f _{AF} = 1 kHz, (main + sub = 90%), AFADJ = 0 dB, PLTADJ = 0 dB		10		%
MPLT _{MIN}	Minimum pilot modulation	L = R = 225 mVrms, f _{AF} = 1 kHz, (main + sub = 90%), AFADJ = 0 dB, PLTADJ = -6 dB		5		%
MPLT _{MAX}	Maximum pilot modulation	L = R = 225 mVrms, f _{AF} = 1 kHz, (main + sub = 90%), AFADJ = 0 dB, PLTADJ = 6 dB		20		%

I²C MODE (BUS_SEL PIN = GND)

I²C Write Data

Table 1. Write Data

BYTE	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
Address	1	1	0	0	0	1	AS	0
Data 1	MUTE	0	N13	N12	N11	N10	N9	N8
Data 2	N7	N6	N5	N4	N3	N2	N1	N0
Data 3	PLTADJ2	PLTADJ1	PLTADJ0	DIS_TX	MONO_ST	TXPOW1	TXPOW0	PORT1
Data 4	PORT2	STBY	BAND	MODADJ3	MODADJ2	MODADJ1	MODADJ0	DIS_AFLPF
Data 5	DIS_EM	EMTC	0	AFADJ2	AFADJ1	AFADJ0	CP1	CP0
Data 6	(reserved) ⁽¹⁾							

(1) Do not write any data on reserved area. The data of this area is loaded at power-on reset.

Table 2. Write Data Symbol Description

SYMBOL	DESCRIPTION		DEFAULT																																				
AS	Address select bit	0: ADD_SEL(POW) pin GND 1: ADD_SEL(POW) pin Open	0																																				
MUTE	Mute control bit	0: Mute off 1: Mute on	0																																				
N13–N0	Programmable counter bits	Set main counter	all 0																																				
PLTADJ2, PLTADJ1, PLTADJ0	Pilot level adjust bits	<table border="1"> <thead> <tr> <th>PLTADJ2</th> <th>PLTADJ1</th> <th>PLTADJ0</th> <th>Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>–6 dB</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>–4 dB</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>–2 dB</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0 dB</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>2 dB</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>4 dB</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>6 dB</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>pilot off</td> </tr> </tbody> </table>	PLTADJ2	PLTADJ1	PLTADJ0	Level	0	0	0	–6 dB	0	0	1	–4 dB	0	1	0	–2 dB	0	1	1	0 dB	1	0	0	2 dB	1	0	1	4 dB	1	1	0	6 dB	1	1	1	pilot off	0, 1, 1
PLTADJ2	PLTADJ1	PLTADJ0	Level																																				
0	0	0	–6 dB																																				
0	0	1	–4 dB																																				
0	1	0	–2 dB																																				
0	1	1	0 dB																																				
1	0	0	2 dB																																				
1	0	1	4 dB																																				
1	1	0	6 dB																																				
1	1	1	pilot off																																				
DIS_TX	Disable TX power amp bit	0: TX power amp on 1: TX power amp off	0																																				
MONO_ST	Mono/stereo switch	0: 38 kHz sub carrier off 1: 38 kHz sub carrier on For mono mode, PLTADJ bits have to be set as "PLTADJ[2:0]=111"	0																																				
TXPOW1, TXPOW0	TX power level selection bits	<table border="1"> <thead> <tr> <th>TXPOW1</th> <th>TXPOW0</th> <th>Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>–7 dBm</td> </tr> <tr> <td>0</td> <td>1</td> <td>–3 dBm</td> </tr> <tr> <td>1</td> <td>0</td> <td>1 dBm</td> </tr> <tr> <td>1</td> <td>1</td> <td>4 dBm</td> </tr> </tbody> </table>	TXPOW1	TXPOW0	Level	0	0	–7 dBm	0	1	–3 dBm	1	0	1 dBm	1	1	4 dBm	0, 0																					
TXPOW1	TXPOW0	Level																																					
0	0	–7 dBm																																					
0	1	–3 dBm																																					
1	0	1 dBm																																					
1	1	4 dBm																																					
PORT1, PORT2	Port control bits	PORT1, PORT2 are enabled as general purpose ports 0: Low (Nch-MOS open drain on) 1: High (Nch-MOS open drain off)	1, 1																																				
STBY	Standby control bit	0: Standby off 1: Standby on	1																																				
BAND	Band selection bit	0: US/EU band (87.5 MHz to 108 MHz) 1: Japan band (76 MHz to 90 MHz)	0																																				

Table 2. Write Data Symbol Description (continued)

SYMBOL	DESCRIPTION					DEFAULT	
MODADJ3– MODADJ0	Modulation adjust bits	MODADJ3	MODADJ2	MODADJ1	MODADJ0	Total Composite Level	
		0	0	0	0	0 dB	
		0	0	0	1	1 dB	
		0	0	1	0	2 dB	
		0	0	1	1	3 dB	
		0	1	0	0	4 dB	
		0	1	0	1	5 dB	
		0	1	1	0	6 dB	
		0	1	1	1	7 dB	
		1	0	0	0	8 dB	
		1	0	0	1	9 dB	
		1	0	1	0	10 dB	
		1	0	1	1	11 dB	
		1	1	0	0	12 dB	
		1	1	0	1	13 dB	
1	1	1	0	14 dB			
1	1	1	1	15 dB			
DIS_AFLPF	Disable 15 kHz LPF	0: AF 15-kHZ LPF enable 1: AF 15-kHZ LPF disable				0	
DIS_EM	Disable pre-emphasis bit	0: De-emphasis on 1: De-emphasis off				0	
EMTC	Time constant control bit for pre-emphasis	0: 50 μ s 1: 75 μ s				1	
AFADJ2, AFADJ1, AFADJ0	AF level adjust bits	<i>AFDJ2</i>	<i>AFDJ1</i>	<i>AFDJ0</i>	<i>Level</i>	0, 1, 1	
		0	0	0	–9 dB		
		0	0	1	–6 dB		
		0	1	0	–3 dB		
		0	1	1	0 dB		
		1	0	0	3 dB		
		1	0	1	6 dB		
		1	1	0	9 dB		
1	1	1	12 dB				
CP1, CP0	CP current selection bits	<i>CP1</i>	<i>CP0</i>	<i>CP Current</i>	1, 0		
		0	0	0.6 μ A			
		0	1	1.25 μ A			
		1	0	2.5 μ A			
		1	1	50 μ A			

PLL Setting in I²C Mode

Calculation of N13–N0 14-bit word (N_{PLL}) can be done as follows:

f_{RF} = desired tuning frequency

f_{XTAL} = crystal frequency (32.768 kHz)

$$N_{PLL} = 4 \times \frac{f_{RF}}{f_{XTAL}}$$

Example:

$f_{RF} = 88.0 \text{ M}$

$$N_{PLL} = 4 \times \frac{88.0 \text{ M}}{32.768 \text{ kHz}} = 10742$$

The PLL word becomes 29F6h (N13, N12, N11, N10, N9, N8, N7, N6, N5, N4, N3, N2, N1, N0 = 10 1001 1111 0110).

Initial setting	Audio input level	L = R = 75 mVrms, AFADJ = 0 dB, $f_s = 400 \text{ Hz}$
	Pilot level:	PLTADJ = 0 dB means 10%
	FM modulation:	MODADJ depends on TX frequency to be 22.5 kHz dev.
	Output power:	TXPOW = –7 dBm, pullup resistance is not necessary
		TXPOW = –3, 1 dBm, antenna load 50 Ω add pullup resistance R_{TX} 300 Ω
		TXPOW = 4 dBm, antenna load 50 Ω add pullup resistance R_{TX} 150 Ω

To Use External XTAL Signal

To use external signal instead of XTAL oscillation, pin assignment is as follows:

- XTAL1 (pin 9): OPEN
- XTAL2 (pin 10): signal input with coupling capacitor

Input signal wave should be sine wave or square wave, acceptable amplitude ranges are:

- Sine wave: 500 mVpp to 2 Vpp
- Rectangle (square) wave: 200 mVpp to 2 Vpp

PARALLEL MODE (BUS_SEL PIN = OPEN)

Channel/Standby Setting in Parallel Mode

CHANNEL SETTING NO.	D4	D3	D2	D1	D0	FREQUENCY (MHz) OR STANDBY	MODADJ SETTING
0	0	0	0	0	0	standby	9
1	0	0	0	0	1	87.7	9
2	0	0	0	1	0	87.9	9
3	0	0	0	1	1	88.1	9
4	0	0	1	0	0	88.3	9
5	0	0	1	0	1	88.5	9
6	0	0	1	1	0	88.7	9
7	0	0	1	1	1	88.9	3
8	0	1	0	0	0	106.7	3
9	0	1	0	0	1	106.9	3
10	0	1	0	1	0	107.1	3
11	0	1	0	1	1	107.3	3
12	0	1	1	0	0	107.5	3
13	0	1	1	0	1	107.7	3
14	0	1	1	1	0	107.9	3
15	0	1	1	1	1	standby	3
16	1	0	0	0	0	standby	13
17	1	0	0	0	1	76.8	13
18	1	0	0	1	0	77.0	13
19	1	0	0	1	1	77.2	13
20	1	0	1	0	0	77.4	13
21	1	0	1	0	1	77.6	13
22	1	0	1	1	0	77.8	13
23	1	0	1	1	1	78.0	13
24	1	1	0	0	0	88.0	9
25	1	1	0	0	1	88.2	9
26	1	1	0	1	0	88.4	9
27	1	1	0	1	1	88.6	9
28	1	1	1	0	0	88.8	9
29	1	1	1	0	1	89.0	9
30	1	1	1	1	0	89.2	9
31	1	1	1	1	1	standby	9

Table 3. TX Power Setting in Parallel Mode

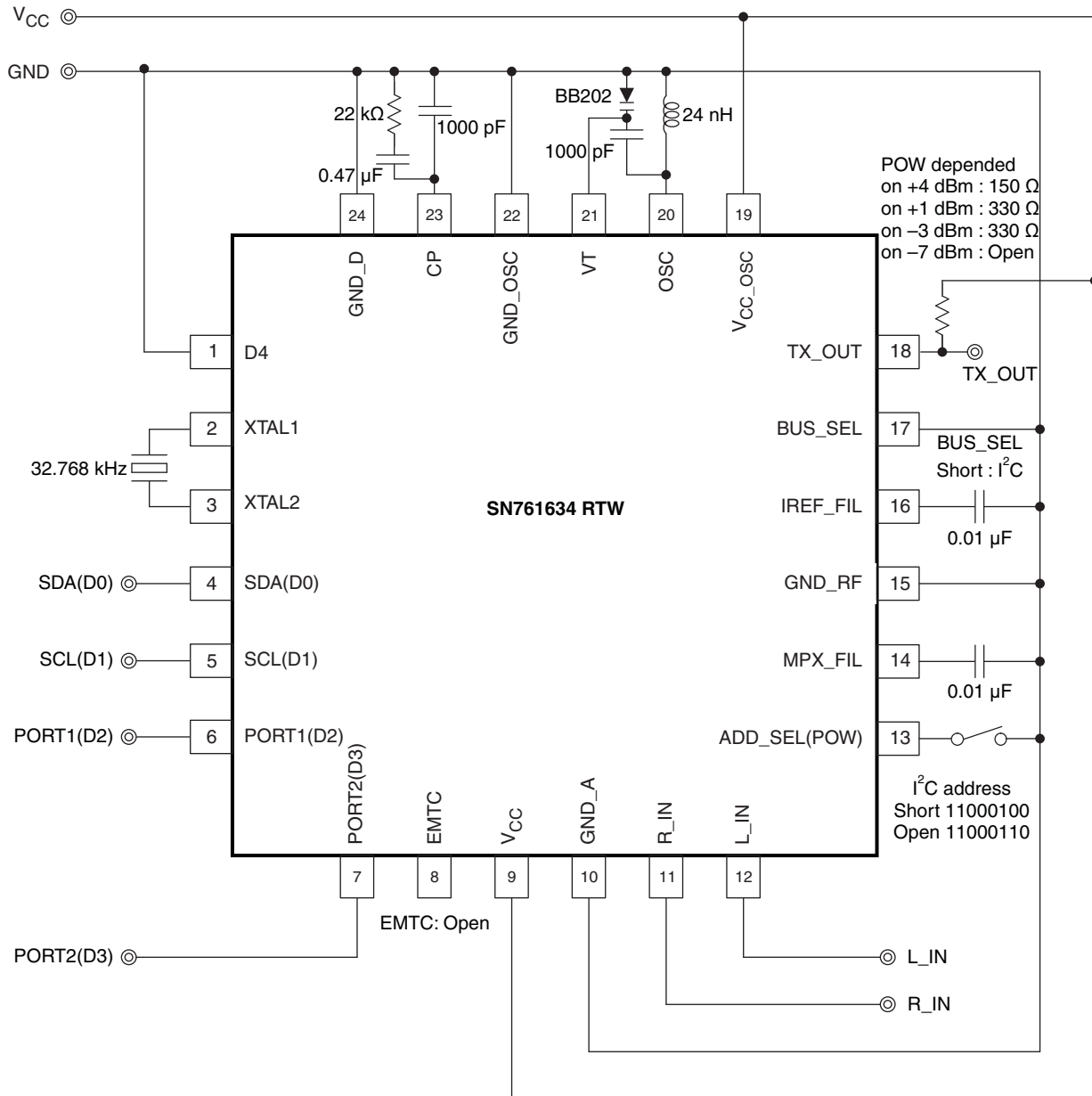
ADD_SEL(POW) PIN	TX POWER
Open	4 dBm
330 k Ω \pm 20% pulldown	1 dBm
100 k Ω \pm 20% pulldown	-3 dBm
GND	-7 dBm

Table 4. Pre-Emphasis Setting in Parallel Mode

EMTC PIN	PRE-EMPHASIS TIME CONSTANT
Open	75 μ s
GND	50 μ s

Other settings used are "default" value in [Table 1](#).

APPLICATION INFORMATION



A. Pin 1 (D4) input connects to GND.

Figure 15. I²C Mode Application

NOTE

This application information is advisory and performance check is required at actual application circuits. TI assumes no responsibility for the consequences of use of this circuit, such as an infringement of intellectual property rights or other rights, including patents, of third parties.

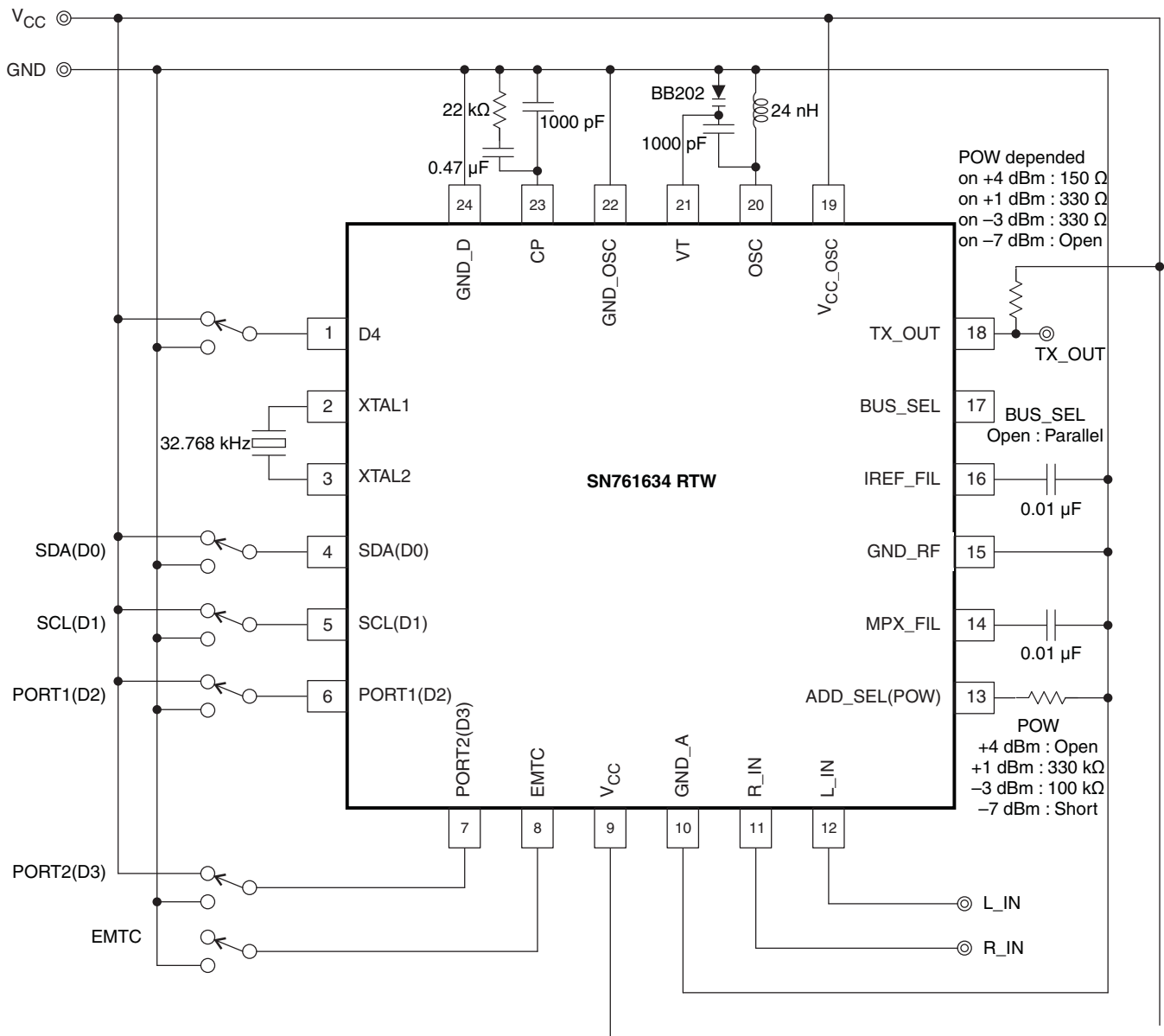


Figure 16. Parallel Mode Application

NOTE

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN761634RTWR	OBSOLETE	WQFN	RTW	24		TBD	Call TI	Call TI	-20 to 85	SN76 1634	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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RTW (S-PWQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4206244/C 07/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-Leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

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